CHARACTERIZATION OF INTEGRATED RESISTORS FOR BROADBAND TELECOM PRINTED CIRCUIT BOARDS

Joris Peeters, Ann Ackaert, Louis Vandam, Koen Allaert, Marnix Botte (*)
Alcatel Bell, Research Division, Components Division (*)

Luc Van den Torren, Luc Martens, Daniël De Zutter
INTEC, University of Gent
Antwerp, Belgium

ABSTRACT

For high speed digital transmission in broadband telecom applications, termination of the interconnection is essential to avoid reflections and inter signal interference in order to minimise bit error rates. Since operating bit rates of 155 and 622 Mbit/s are common nowadays for ATM switching, a lot of attention is paid to all kinds of parasitic effects that deteriorate the termination resistance value in the high frequency range. It should be possible to substantially improve the quality of the line termination by integrating the resistors into the printed circuit board and by locating the termination very close to the component pin. In addition, by reducing the board area which is normally occupied by surface mount termination resistors, active components can be placed closer together. Reduction of the line length gives rise to improved performance of the interconnection network and higher active component density yields a higher functionality of the board.

A test board was realised for processing characterization and reliability evaluation of the integrated resistor technology within multilayer printed circuit boards. Test structures are included to characterise the impedance of the integrated resistors at high frequencies in order to evaluate the resistors for use in high speed broadband telecom boards. In addition, high precision etching tests are performed to determine and optimise the tolerance on the resistance values.

High frequency measurements were performed up to 5 GHz using a Network Analyser HP5810C. Test structures were connected by means of coplanar ground-signal probes. Calibration structures allow to perform de-embedding on the measured characteristics. From the measurements, an equivalent network was extracted which perfectly matches the resistor characteristics within the relevant frequency range.

Since reliability of new technologies is a critical issue within telecom applications, the integrated resistor modules were subjected to several environmental stress tests, including damp heat, thermocycling and ageing with and without load. Measured resistor characteristics were clearly better than the material specifications for maximum resistor deviation, often as much as one order of magnitude. Ageing tests under loading conditions allowed to specify maximum heat dissipation densities. From processing characterization data and dissipation density limits, design rules for minimum resistor dimensions were derived.

INTRODUCTION

The tendency for increasing integration of passive discrete components into the interconnection substrate is well known for thick film hybrid and for thin film technologies. Also for printed circuit boards there is a possibility to integrate surface mount discrete resistors and capacitors into the board, making use of a buried planar resistor or capacitor technology. Not only board densification is achieved in this way, but, which is more important in case of high speed / high performance telecom boards, the electrical characteristics of the integrated device can be fairly improved with respect to its surface mount counterpart.

This paper focuses on the integration of resistors into PCB's. Among different available technologies, a thin film technology for integration of resistors was selected for further evaluation. This technology consists of a Cu foil on which a resistive layer is deposited. The special foil can be cladded with various types of laminate materials [1,2,3]. For easy implementation of such a technology, it is important that the number specific processing steps is limited as much as possible in order to reduce the impact on the standard processing flow. Resistors are defined by means of a number of subsequent etching steps.

Section 2 describes a test board which has been realised for process evaluation, high frequency characterisation and reliability testing. An overview of the process characterisation and parameter extraction is provided in section 3. High frequency characterisation is the subject of section 4. The following section deals with the results of environmental stress tests to evaluate the reliability of the technology. From the characterisation results for the first test vehicle processing run, design rules are derived in section 6. Section 7 deals with the impact of resistor integration on PCB design and lay-out. Specific application areas where much benefit of the technology is expected are described. Conclusions and future work are discussed in Section 8.

INTEGRATED RESISTOR TEST VEHICLE

A joined co-operation with the University of Gent was set up in order to realise a test board for processing characterisation and reliability evaluation of the integrated resistor technology within multi-layer printed circuit boards. Test structures are included to characterise the impedance of the integrated resistors at high frequencies in order to evaluate the resistors for use in high speed broadband telecom boards.

Figure 1 shows schematically the built-up of the test board. Typical line width is 125 µm. Layer thickness of laminate and prepreg is chosen in such a way that a characteristic impedance of 50 Ω is obtained throughout the board for all microstrips and striplines

connecting the resistors. In this way, accurate characterisation of the resistance value is possible up to high frequencies using S-parameter measurements. The multi-layer test board includes 3 internal layers of Ohmega-ply, respectively of 25, 100 and 250 Ω/□. Normally, the material was purchased with a Cu foil of 17.5 µm. Only for the 250 Ω/□, Cu thickness was 35 µm. It will be made clear that the lower the Cu thickness is, the more accurately the resistor can be defined.

Resistors are always located at reference levels (GND or VDD planes in actual designs). This will allow improved cooling of the resistors because of the large amount of Cu in the neighbourhood, and the resistors do not interfere with the routing on the interconnection layers. The complete test vehicle built-up also provides resistors implemented on the top layer (outer layer) of the board. So far, these resistors have not been included on test vehicles that were realised.

The test board lay-out can be subdivided in three parts. A first part (HF module) aims at high frequency characterisation of the resistors. Resistance value is in the range of 50 to 150 Ω, which is typical for serial and parallel termination resistors for single and differential interconnections for high speed digital signals. Both serial and grounded resistors are included. A second area (DC1 module) is provided for DC characterisation of the technology by means of high precision 4-point resistor measurements. By means of a wide range of resistance values (from 10 Ω up to several k Ω's) and several values of the resistor width (from 150 to 600

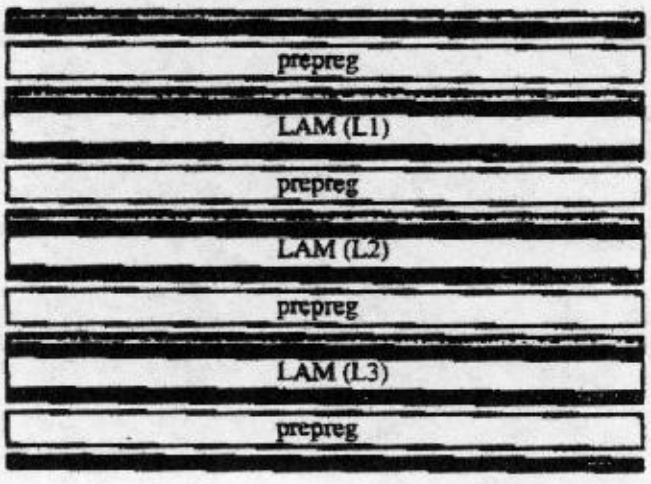

Figure 1. Built-up of the integrated resistor multilayer test board

µm) it is possible to precisely characterise and optimise the different processing steps for the integrated resistors. A third area (DC2 module) of the test board is designed to perform thermal stress measurements for evaluation of the process reliability of the technology. All resistors on this particular module have a width of 600 µm.

PROCESS CHARACTERISATION

DC 4-point measurements were performed on the modules DC1 and DC2 of 4 test boards. The goal is a precise characterisation of the actual resistance value for the different materials and for different resistor dimensions. The influence of material and dimensional parameters on the resistance value is determined. Approximate figures of reproducibility and uniformity are estimated. The number of measurements and the number of test boards is however too small to perform a complete statistical analysis.

Without exception, the actual measured resistance values are higher than the design values. This resistance increase is caused by a modification of the resistor geometry due to underetching, combined with a deviation of the square resistance. Uniformity and reproducibility of the square resistance are determined by the quality of the basic material (which has a tolerance guarantee of of ± 5 % [4]) and possible damaging effects due to non-selectivity during the resistor etching process. Typical values for average and standard deviation of the resistance values (deviation with respect to design values) and extracted parameters for width, length and square resistance are summarised in table 1.

Table 1 shows that good results were obtained for low ohmic materials, while for the 250 Ω/□ material a high increase of the sheet resistance was noticed, which could not be explained properly up till now. For the low ohmic materials, an absolute tolerance specification of ± 10 % for the resistance value with respect to the design value was not accomplished yet. A differential tolerance of ± 10 % could however be achieved. The extracted underetching parameters however allow to implement correct spreads on the artwork. Figures 2 shows for example the measured resistance deviation for all resistors of the DC2 modules, which were realised using the 100 Ω/□ material. In addition, the simulated resistance deviation is shown after theoretical compensation of the underetch figures specified in table 1. This clearly indicates that, when appropriate corrections are performed to the artwork and some improvement is obtained for the process uniformity, it will be possible to end up within the ± 10 % absolute tolerance window for the investigated low ohmic materials.

Table 1. Typical values for average resistor increase and standard deviation, and parameter extraction results for changes of resistor length and width and square resistance.

	Measurements		**Parameter extraction**		
Sq. resistance (Ω/□)	Av. increase (%)	St. deviation (%)	Sq. Resistance (Ω/□)	Delta L (µm)	Delta W (µm)
25	11	3	25,8	80	25
100	7,5	3,5	98	50	35
250	40	5	325	120	28

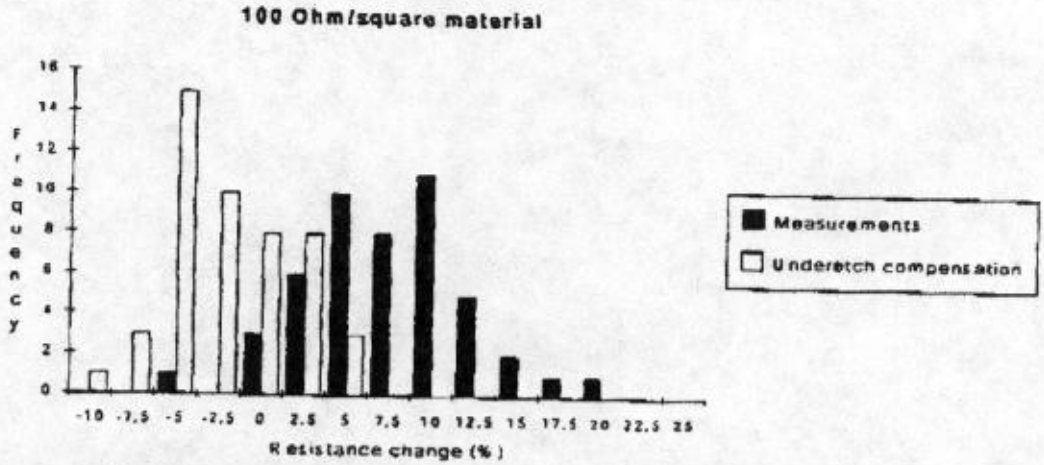

Figure 2. Measured resistance deviation for the 100 Ω/□ resistors of the DC2 modules and simulated resistance deviation after theoretical underetch compensation

HIGH FREQUENCY CHARACTERISATION

To be a candidate for line termination of high-speed digital interconnections in broad-band telecommunication systems, two questions have to be answered:

1) Is the resistor frequency-independent within the relevant frequency range for the considered application (for broad-band transmission at a rate of 620 Mbit/s the relevant bandwidth is 3 GHz) ?

2) What is the magnitude of the effect of the parasitic capacitances and inductances ?

Figure 3 shows a test configuration for high frequency measurements on the test board. The left-hand side of the figure shows the probe pads (signal contact and ground contact provided through a via hole contacting the ground plane) on which a coplanar package signal-ground probe is placed that connects the test structure with the coaxial inputs of a network analyser (HP 8510C). At the right-hand side of the figure an integrated resistor is placed in the gap between the signal via hole and the ground plane. The test board is mounted on a board-probing station which allows to accurately position the package probes on the different test structures [5]. The measurements were performed in the frequency range 45 MHz - 5 GHz. For termination resistors, one-port measurements have been done while feed-through resistors are characterised by a two-port S-matrix.

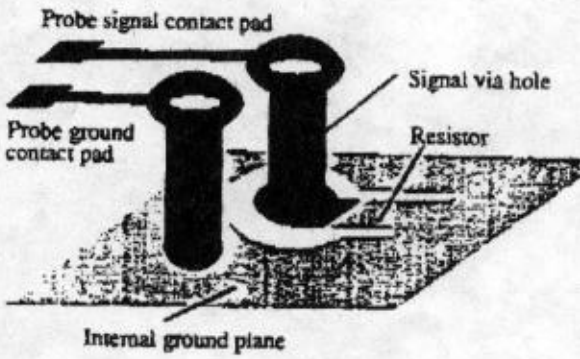

Figure 3. Measurement set-up for high frequency characterisation of integrated resistors using a coplanar probe

In order to determine the inherent characteristics of the integrated resistor, the influence of the test fixture must be removed. This has been done by calibrating the measurements at the tip of the probe using standard loads on a ceramic standard substrate. For one-port measurements a 50 Ω resistor, a short-circuit and an open-circuit are used. To determine the influence of the probe pads, the signal line and the signal via hole, additional test structures are provided. The method of de-embedding can be used to extract the behaviour of these parts of the test structure from the measurement results.

To better understand the high-frequency behaviour, the S-parameters obtained after de-embedding of the probe contacts and the signal lines from the measured ones were converted to a circuit model. The parameters of this model were estimated on the

basis of the measurements. Figure 4 shows such a model for the test structure of figure 3. The inductance is due to the via hole and the main contribution to the capacitance comes from the gap between the via hole and the ground plane. This was confirmed by a measurement on the same configuration of figure 3 but with a short-circuit replacing the resistor. One can conclude that a better design of the via hole can reduce the parasitics and improve the performance of the integrated resistor.

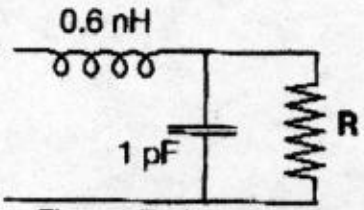

Figure 4. Equivalent network for an integrated resistor up to a frequency of 5 GHz

The model parameters have been determined for resistors in 25, 100 and 250 Ω/□ materials. The number of squares of the resistor area was limited, because the termination typically requires low-ohmic values (in between 50 and 150 Ω). Four resistor values were designed: 50, 75, 100 and 150 Ω. It turned out that the resistor characteristics could perfectly be matched by the equivalent circuit model of figure 4 in the considered frequency range. For all resistors, the resistance was frequency independent and equal to the DC-value and the parasitics were relatively small: typical values of respectively 1 pF and 0.6 nH were obtained for the capacitance and the inductance. Table 2 gives a summary of minimum and maximum values for different square resistance values.

It should be noted that, nevertheless the parasitic effects are small compared to those of traditional surface mount resistors, they already cause a rather important degradation of the "total" resistance characteristics at high frequencies. With the typical figures of the parasitics, the real part of the input impedance at 5 GHz can differ from the DC-value over more than 50 %. This again shows that a controlled design of the via hole necessary for a good high-frequency performance.

Table 2. Minimum and maximum parasitic effects extracted from measured characteristics of integrated resistors.

Layer (Ω/□)	Lmin (nH)	Lmax (nH)	Cmin (pF)	Cmax (pF)
25	0.599	0.657	0.935	1.139
100	0.622	0.682	1.053	1.154
250	0.571	0.653	1.117	1.202
short	0.6		1	

RELIABILITY AND ENVIRONMENTAL STRESS TESTS.

Four DC2 modules were used to perform reliability and environmental stress tests. The number of measured devices was too small to perform a complete statistical analysis for qualification of the technology, but allowed to verify the data which are specified by the material supplier and to compare them with characteristics of discete resistors. All resistance measurements were 4-point ones. Table 3 gives an overview of the tests performed on modules 1 till 3. The measurement results are shown and comparison is made with the manufacturer specifications. The measurments are also compared to the performance of discrete thick film chip resistors of size 0805. On module 4, an ageing test under loading conditions was performed. For this purpose all resistors were connected to a voltage supply of 5V for 2000 hours, without temperature cycling. In this way the power dissipation depends on the value of the resistor. The combined results for the 3 examined materials are shown in figure 12. The (relative) resistance change is expressed here as a function of the power density. The test is extremely severe for small resistors, reduced resistor area and low sheet resistance. The manufacturer specifications for maximum thermal dissipation and ageing conditions are summarised in table 4.

Table 3. Summary of reliability and environmental stress tests : comparison with specifications of the material supplier and performance of 125 mW discrete thick film chip resistors of size 0805 (size : 2 mm x 1.25 mm) [6]

Mod. nr.	Test	Measured max. / min. ΔR	Specification of material supplier	Thick film chip R (0805)
1	**Humidity test** **40 °C / 93 % RV**	**After 21 days :** 0.22 % for 25 Ω/□ 0.07 % for 100 Ω/□ 0.10 % for 250 Ω/□ **After 56 days :** 0.74 % for 25 Ω/□ 0.14 % for 100 Ω/□ 0.22 % for 250 Ω/□	**After 10 days :** 0.5 % for 25 Ω/□ 1 % for 100 Ω/□	**After 56 days :** ≤ ± 1.5 %
2	**Thermal cycling** **-25 °C / 125 °C**	**After 100 cycles :** -0.03 % for 25 Ω/□ 0.03 % for 100 Ω/□ -0.08 % for 250 Ω/□	**After 25 cycles :** -0.5 % for 25 Ω/□ 1 % for 100 Ω/□	≤ ± 0.25 %
2	**Ageing without load** **125 °C, 1000 hours**	0.10 % for 25 Ω/□ 0.08 % for 100 Ω/□ -0.13 % for 250 Ω/□	not specified	not specified
3	**Solder heat** **260 °C,** **immersion 20 s**	-0.02 % for 25 Ω/□ -0.01 % for 100 Ω/□ 0.01 % for 250 Ω/□	0.5 % for 25 Ω/□ 1 % for 100 Ω/□	≤ ± 0.25 %

Table 4. Summary of reliability and environmental stress tests ; comparison with material supplier specifications

Material (Ω/□)	Allowed thermal dissipation (mW/mm²)	Resistance change after loaded ageing (1000 hours, 70 °C ambient)
25	>240	2% maximum (with 8 mW/mm² load)
100	>120	3% maximum (with 4 mW/mm² load)
250	>120	1% maximum (with 4 mW/mm²load)

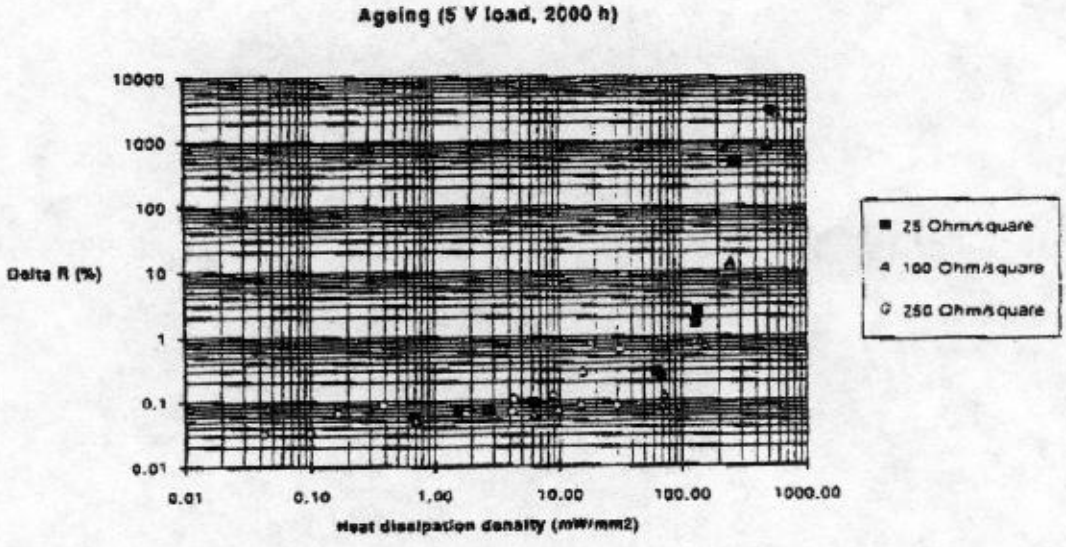

Figure 5. Ageing under load conditions : ΔR as a function of the heat dissipation density

Figure 5 shows that the relative change of the resistance on the DC2 module for 4 to 8 mW/mm² heat dissipation density is in the range of 0.1 %, which is clearly better than the material specifications. It can also be noticed that, without special precautions, a heat dissipation density of 240 mW/mm², even for the 25 Ω/□ material will lead to unrecoverable damage of the resistor material. In this particular test vehicle, a natural heat sink was present in the form of a continuous ground plane, but was clearly not sufficient for the resistor cooling. According to figure 5, a maximum power dissipation density of 100 mW/mm² seems to be more appropriate. In the next section this will be worked out further to come to a first guideline for minimum lay-out rules for the resistors.

A comparison between the measurement results for integrated resistors and the performance of discrete resistors (125 mW, size 0805), as specified in table 3, shows that in terms of reliability, integrated resistors can easily compete with discrete resistors. For 1000 hours ageing with load at 70° C ambient, a maximum change of 1 % is specified for the 0805 components. Figure 5 shows that, if a dissipation density of 100 mW/mm² is not exceeded, the same performance can be expected for integrated resistors.

It can be concluded that for all reliability and environmental stress tests (damp heat, thermocycling, solder float, ageing with and without load) measured resistor characteristics were clearly better than the material specifications for maximum resistor deviation, often as much as one order of magnitude. On the DC2 module, resistors were provided with and without a thermal insulation. A thermal insulation would not only reduce thermal flow from the outer board layers (during assembly) via through holes towards the resistors, but also would prevent harmful environmental influences (chemical, mechanical,...) from migrating to the resistors. It was concluded that this thermal insulation however did not really affect the results of the reliability tests.

LAYOUT RULES FOR INTEGRATED RESISTOR DESIGN

Integrated resistor design starts with the choice of an appropriate sheet resistance. Next, a minimum resistor dimension is determined, which actually is the subject of this section. A minimum square has its sides (width and length) equal to this minimum dimension resistor of this shape is actually the smallest resistor which can be realised, with a value equal to the sheet resistance of the layer. Larger resistor values are realised by lay-outing a number of squares in series (length of the resistor is larger than the width), smaller resistors have several squares in parallel (width of the resistor is larger than the length).

Specifications for minimum lay-out rules originate from two sources, the processing capability of the PCB manufacturer and the allowable heat dissipation density. With regards to processing capability, minimum lay-out rules are generated starting from the tolerance level on the resistance value that has to be achieved. Since there is a certain spread on the underetching, a tolerance level must be specified for the width and length of the resistor. It is clear that, for a given variability of the underetching, the effect on the resistor tolerance is larger for resistors with small dimensions than for resistors with large dimensions. The resistor which is affected most is the one which consists of only one square, with a value equal to the sheet resistance. It is evident that the minimum lay-out rules for the complete resistor layer should be based on the resistor with the smallest dimensions, being (in general) the 'one square' resistor. Remark that a difference is made here between minimum size (= one square) and minimum value (several squares in parallel) !

Suppose that the tolerance on the sheet resistance equals ± 5 % (material specifications). Let us assume also that resistor processing has only a minor effect on this tolerance level (which was demonstrated for the 25 and 100 Ω/□ materials in the test vehicle). It can be verified that, in case of equal underetch tolerance for both width and length of the resistor, this tolerance should be within ± 2.5 % of the resistor (square) side. Let us assume further that the underetching variability equals the average amount of underetching, which on its turn is equal to the thickness of the metal layer that is etched (divided equally between the two sides of the etched pattern). This means that ± 2.5 % of the resistor side should be at least equal to the thickness of the Cu layer on top of the resistive layer. For 17.5 µm Cu thickness, the minimum square size becomes 20 times the Cu thickness, or 350 µm. For 35 µm Cu thickness, the minimum size becomes 700 µm. If the minimum resistor value corresponds to two squares (for example 50 Ω resistor realised in a 25 Ω/□ layer), an underetch tolerance of ± 3 % of the square side can be tolerated, yielding a minimum square dimension of 300 µm in case of 17.5 µm thick Cu. The 50 Ω resistor will have a width of 300 µm and a length of 600 µm. It is guaranteed that any resistor with a larger value has coarser tolerance specs compared to the minimum size (one square) resistor.

The second source for minimum lay-out rules for integrated resistors comes from thermal dissipation. The base for this was explained in the preceding sections, where figure 5 showed resistance deviation due to ageing under load conditions, as a function of the thermal dissipation density. A density limit of 100 mW/mm² has been established at that time. The power dissipation spec for discrete resistors in telecom (small band and broad band) equals 125 mW. For integrated resistors, minimum resistor area consequently becomes 1.25 mm². Suppose for example that a 50 Ω resistor is realised in a 25 Ω/□ layer, 2 squares are required. Taking into account minimum resistor area, each square must have an area of 0.625 mm². This yields a minimum square side dimension of 800 µm. The width of the resistor is equal to this minimum size, its length is twice the minimum size. A 100 Ω resistor realised in the same layer, consists of 4 squares, each with an area of 0.2 mm². This yields a minimum resistor width of 450 µm

In addition, 'burn through current' measurements were performed on resistors of various size and sheet resistance. For a particular sheet resistance, a linear relationship was detected between the width of a resistor and the failure current. The extracted failure currents were in line with the results of the ageing test under load conditions. The heat dissipation density which corresponds to the failure currents were well above the limit of 100 mW/mm².

It has to be remarked that for termination resistors at present conditions the minimum lay-out rules which originate from thermal dissipation limits are more severe than those directed by underetching variability. Consequently, in the near future, effort should not go to improvement of processing capabilities, but to increased thermal performance of the material. One way might be the reduction of the power supply voltage down to 3.3 V, which most probably will reduce the power dissipation spec of 125 mW. Another way is to look at the use of heat sinks in the neighbourhood of the resistors. The realisation of the resistors in a thick Cu reference plane has its benefits for cooling, but harms the tolerance level of the etching process. It even has to be questioned whether the 'requirement' of only 1 % deviation of the resistance value over its life time is not too severe. Also for discrete resistors, the power dissipation spec becomes a problem if the present miniaturisation trend continues. Resistors of size 0603 are qualified in general up to 100 mW, size 0402 only allows 63 mW [6].

CONSEQUENCES OF RESISTOR INTEGRATION FOR PRINTED BOARD DESIGN AND LAY-OUT

On high speed line termination and switching boards for broad band telecommunications traditionally a zone of 1 cm width around each ASIC is occupied for mounting the required discrete resistors and capacitors on the component side and solder side of the board. The dimensions of these components in production is presently typically 2 mm by 1.25 mm (size 0805 components). The size of integrated resistors is only limited by heat dissipation density and the feature size of the printed board technology, and compared to discrete resistors, they certainly will consume less area. Considering the fact that integrated resistors can also be placed underneath the IC, it is clear that integration allows to place the termination much closer to the IC pin than in case of surface mounting.

Especially in case of area array packages, integration of resistors is highly beneficial. Suppose that for example a ball grid array package would be combined with surface mount chip resistors for the termination of high speed interconnections. In BGA footprints, most solder pads are directly connected to a via and signal distribution is taken care of on internal wiring planes. Figure 14 shows that this implies that for each termination resistor, two additional via holes are required for connection of this resistor in a peripheral area around the BGA. The density benefit of area array packages would be completely offset. For a PQFP 208 with 0.5 mm pitch (area of 1000 mm²), a total of 100 discrete components occupy an area in excess of 650 mm² (without routing or vias). In case of a 208 I/O BGA with full array, only the outside rows of pads can be connected on the component or solder side of the board. The central part of the grid needs vias for connection on inner layers. In case of TH's, the counter side of the board does not offer room for discrete component location. Although the introduction of BGA's induce an important component area reduction (500 mm² for 208 I/O's and 1.5 mm grid pitch) the mounting area for discrete components and TH's for connecting these components will offset the potential area saving. The use of integrated resistors allow to embed the resistors into the BGA footprint in between the TH's (see figure 6). The density advantage of resistor integration will be even more evident in the future, when flip-chip attach becomes viable as assembly technology for printed circuit boards.

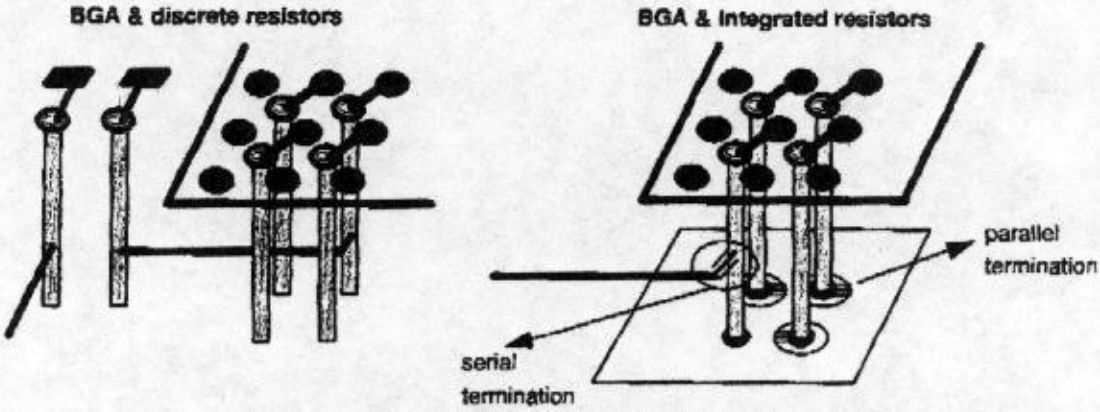

Figure 6. Benefit of integrated resistors for area array components

The dense concentration of termination resistors around the package pads has several advantages. Board area is saved, allowing to increase the density of active devices. Perhaps more important, if one considers present bit rates up to 155 and 622 MBit/s on broad band telecommunication boards, is the reduction of the inductance of the termination resistor (see section 4). An additional advantage of resistor integration is a higher (first pass) yield forecast since fewer solder joints are needed.

The question whether integration of resistors would yield a reduction of the number of via connections, was addressed in detail in [1].

Resistors can be realised on inner layers, signal or reference planes, or outer layers. For inner layers, realising the integrated resistors on a reference plane offers improved heat spreading for dissipation in the termination due to the large amount of Cu in the direct neighbourhood of the resistor and avoids interference with the routing. Via's are saved in case of parallel termination.

Resistors embedded on outer layers have the advantage that vias can be saved in case of serial line termination. Air flow might improve tolerated heat dissipation, however this has to be verified by means of thermal simulations. With a visible resistor on the outer layer also some actions for engineering debugging remain possible. Disadvantages of this resistor location is its increased vulnerability (only protected by solder resist from thermal, mechanical and chemical influences) and the fact that the resistor has to be defined in thick electroplated Cu. Increased Cu thickness means an increase of the etching tolerance and consequently larger minimum lay-out rules. In addition, since there is a certain tolerance on the plating thickness, the selective etching of Cu on top of the resistive layer is less controllable.

The major issue of the integrated resistor technology still is the tolerance of ± 10 % on the resistance value with respect to the design value. It is clear that, without laser trimming corrections, integrated resistors will never be able to compete with the 1 % tolerance which is offered by discrete thick film chip resistors (although for further miniaturisation of surface mount resistors down to size 0402 the tolerance will increase up to 2 % and perhaps even 5 %).

It can however be questioned whether it is really necessary to handle such severe tolerance values for the DC value of termination resistors. In fact, it was clearly demonstrated in section 4 that the DC tolerance of integrated resistors is small if compared to the vast effects that the parasitic inductance and capacitance of discrete resistance have on the termination resistance at high frequencies. And it is evident that line termination should focus in the first place on the high frequency content of the signal ...

CONCLUSIONS AND FUTURE WORK

Out of the characterisation results of test boards with integrated resistors, a number of benefits with respect to traditional SMD resistor assembly technology could be demonstrated :

- Reduction of the parasitic effects at high frequencies of the path towards a (termination) resistor. Although actually no comparison was made between integrated and SMD resistors at high frequencies, the advantage of integrated resistors can be easily proved looking at the characterisation results.

- The reliability of the integrated resistors, which is in fact very much comparable to SMD resistors.

- The fact that it is possible to reduce resistor dimensions as such by integrating them. By realising the resistors on inner layers, additional board area is made free for assembly of active components or board size reduction

- The fundamental advantage that integration provides in case of area array components such as ball grid arrays and full array flip-chip. For each component, a large number of through holes can be avoided and routing can be simplified seriously.

Several issues of the technology however remain :

- The tolerance on the resistor value (± 10 %) is large if compared to what is presently offered by discrete components. However, at high frequencies, because of their low parasitic capacitive and inductive effects, integrated resistors most probably will match better with the characteristic line impedance that discrete terminations do. In addition, it can be questioned whether this low tolerances can be maintained for discretes in case of continuous miniaturisation....

- Present specifications for maximum tolerable heat dissipation limit further size reduction of the integrated resistors for low resistance values. In case of a reduced power supply voltage, it should however be possible to review the heat dissipation specification . Also for very small discrete resistors, the present specification of 125 mW will be a problem.

Further study of these issues is mandatory. Future actions will involve the improve of the resistance stability at high dissipation densities, implementation of appropriate correction factors in the artwork, evaluation of resistor processing on outer layers and adaptation of PCB CAD software to accommodate for the use of integrated resistors

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