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Planar Resistor Technology for High-Speed Multilayer Boards

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Planar resistors incorporated into an internal plane of a circuit board are especially attractive for ECL designs.

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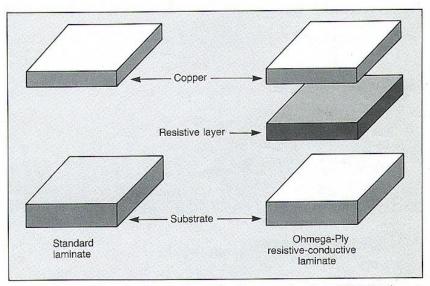
Planar resistor technology is a thinfilm resistor system suited for highspeed and high-density multilayer applications. Utilizing standard subtractive printed circuit board techniques, it is used in various analog and digital applications, from surface resistor potentiometers in consumer electronics to terminating resistors on internal planes of multilayer boards.

This article describes Ohmega's planar resistor technology, its use in high-speed and high-frequency applications, and provides details of the evaluation and use of this technology by Cray Research, a supercomputer manufacturer based in Chippewa Falls, Wisc.

Material characteristics

The laminate system consists of an insulating substrate and, rather than a single conductive layer, a two-layer bifunctional cladding (Fig. 1). The lower layer, immediately against the base laminate surface, is an electrically resistive material. The upper layer is copper. The two layers of this bifunctional cladding are in contact with each other over their entire area. By means of a selective etching, the two layers can be etched differentially so that separate patterns of conductors and resistors are formed (Fig. 2).

Since the resistive material is a thin film (4 to 16 μ in. depending on sheet resistivity), the resulting circuits are essentially two-dimensional. The film thickness is fixed when the resistor-conductor laminate is manufactured and is not a fabrication variable. In determining resistor value, the sheet resistivity is the most important de-



1. The laminate system for planar resistor technology uses a two-layer, bifunctional cladding.

sign parameter. The sheet resistances of available Ohmega-Ply materials are 25 $\Omega/{\rm sq}$ and 100 $\Omega/{\rm sq}.$

Any square resistor will have a value equal to the sheet resistance. To get higher resistor values, the number of "squares" must be increased. A resistor with a high value would be long and narrow; a low-value resistor would be short and wide. In higher values, a long and narrow resistor is usually serpentined to minimize the board real estate used.

Planar resistor applications

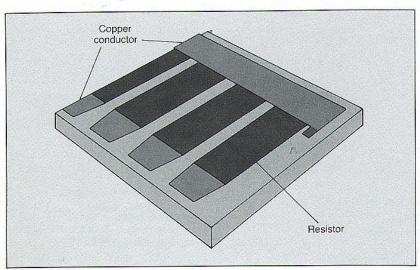
Because of their thin film, planar nature, the resistors can be incorporated into the internal plane of printed circuit boards. This multilayer approach eliminates surface resistors. It is especially effective for computer logic designs such as emitter-coupled logic (ECL), in which large numbers of

terminating resistors are required. Advantages of using this type of resistive system include:

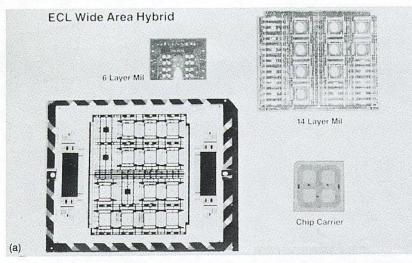
• Increased circuit density. With resistive elements in, rather than on the board, board real estate becomes available which would have normally been provided for the resistors. This allows either the design of a smaller, more dense board, or the increase in the number of logic packages on the board.

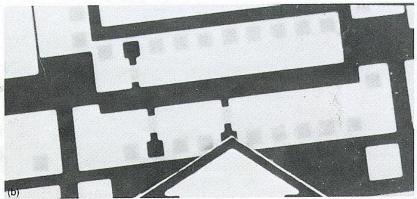
• Improved reliability. With fewer through holes (necessary for discrete or SIP resistors) and solder joints (necessary for chip as well as through-hole attachment) reliability increases, since fewer mechanical connections are required. The chance that a resistor is incorrectly assembled or the wrong resistor used in assembly is also eliminated.

Improved electrical properties. Resistors buried internally are connected



2. Selective etching of the two-layer cladding forms different patterns of conductors and resistors.





3. High-temperature substrate systems using planar resistor technology are shown in (a). Terminating resistors on an internal plane of the 14-layer board are shown in (b).

to the IC lead using the same through hole or via that is used for the IC package attachment. This improves the proximity of the resistor to the IC, therefore improving impedence matching and reducing line delay. Being essentially thin film, the resistors do not show the inductive characteristics of discrete resistors.

• Cost reduction by increasing manufacturing automation. By producing resistors at the same time as the other inner layers of the multilayer board, the need for inventory and assembly of resistors is eliminated.

Since surface-mount technology is attempting to address the need for greater circuit densities, while at the same time trying to reduce manufacturing and assembly costs, planar resistor technology becomes a very complementary technology. In addition, the number of resistors produced on any given unit of area is only a function of the design requirements. The material (and printed circuit) costs for producing 10 resistors or 1,000 resistors on one board are the same.

Examples of specific circuit boards that incorporate planar resistor technology illustrate application areas. One multilayer board design (eight layers, 17 in. by 21 in.) uses planar resistor technology on an internal voltage plane for terminating resistors. Built by VAL Circuits, Santa Ana, Calif., the board is used by Harris Computer Systems Division in their H-1000 superminicomputer.

Another printed circuit board design contains pull-up resistors for a mixed logic application. By using planar resistor technology, designers increased the number of active components on the surface of the board without having to increase the board size. This particular board is an IBM soft card manufactured by Harris Data Communications to tie-in the IBM personal computer to their office automation equipment.

Figure 3 shows circuits which utilize the technology in conjunction with high-temperature substrate systems, specifically triazine-glass and polyimide-glass. These particular circuits, built by Qualitron Corp., Danbury, Conn., are for military applications.

An enlarged photograph of the internal plane of the 14-layer board shows some of the terminating resistors. The pad areas with black oxide will be drilled and plated through for inser-

tion of the legs of IC packages. Signal propagation will thus be through the IC leg, through the terminating resistor and into the -2 V plane. The proximity of the terminating resistor to the end of the drive line improves impedence matching and reduces line delay, resulting in better overall sys-

tem performance.

With the advent of surface-mount technology, there has been much industry attention focused on development of substrates with low coefficient of thermal expansion for use with leadless, ceramic chip carriers. Figure 4 is one such multilayer test board made of polyimide-quartz and containing 68lead JEDEC type C, leadless, ceramic

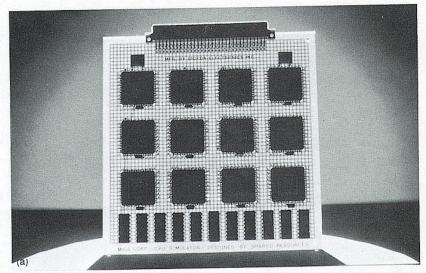
chip carriers.

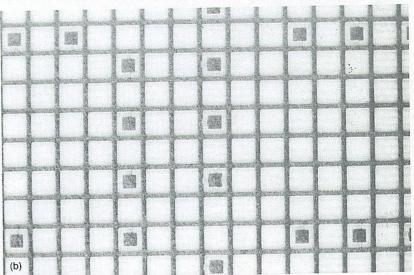
The inner layer of the test board contains planar resistors. An enlarged photograph of that inner layer shows the resistive elements actually designed into the clearance area surrounding the interconnect pads. Note also the removal of an excess of the copper plane. This was done to minimize the expansion effect of the copper plane on the overall package. Currently, planar resistor technology in conjunction with polyimide-quartz is designed into a system specifically because the low dielectric constant (approximately 3.0) and low loss of the quartz substrate is attractive for the required operating frequencies.

At higher frequencies, the use of low-loss substrates such as PTFE is preferred. The resistor system can be operated at very high frequencies. The planar nature of the resistive film eliminates the inductance realized by chip resistors in high-frequency stripline applications.

Material properties

The power dissipation of the resistive element is a function of the resistor size and the maximum hot-spot temperature plus ambient temperature of the resistor element. Power dissipation is substrate limiting. For example, if a resistor were operated in 100°C ambient, and, with power applied, the resistor demonstrated a 50°C temperature rise, the maximum hot spot of the resistor would actually be 100°C ambient plus 50°C, or 150°C. If the substrate were epoxy-glass FR-4, continuous operation would cause the resin to degrade and the thin-film resistor to lose structural support, resulting in resistor value instability.





4. Polyimide-quartz board with leadless, ceramic chip carriers (a) contains planar resistors on an inner layer (b).

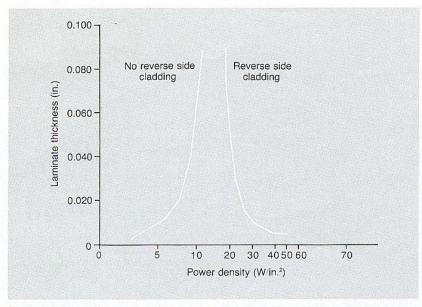
This is discussed later in some Cray Research data.

Figure 5 shows the power dissipation for a resistor element 0.5-in. long and 0.05-in. wide. The resistor element is on the surface of the FR-4 substrate. Ambient is 70°C. The maximum power density to increase the resistor operating temperature to 125°C is plotted. As can be seen, the use of heat sinking, in this case reverse side cladding with 1-oz copper, can greatly increase the power density by allowing the removal of heat from the resistor hot-spot area.

The characteristic properties of planar resistors, when designed onto an internal plane of a multilayer board, were determined with test circuits manufactured by Ohmega Technologies. For one specific test circuit the design specifications were:

- A. Substrate: Epoxy-glass (FR-4) B. Dimensions: 4.5 in. by 4.5 in., 0.062-in. thick
- C. Number of layers: 4
- D. Layer identification: Layer 1 — Signal plane, 1-oz copper Layer 2 — Split power, 1-oz copper

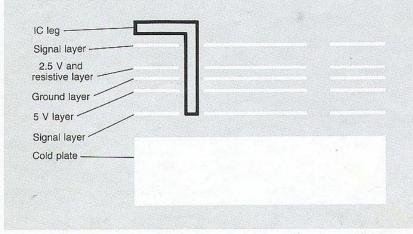
(includes Ohmega resistors) Layer 3 - Ground plane, 1-oz



5. Heat sinking with copper cladding removes heat from the resistor hot-spot area.

ECL test circuit results	
	Average ∆R (%)
Hot oil (96 resistors)	
IPC method 2.4.6: 260°C, 20 s	-0.1
Soldering, heat (96 resistors)	
MIL-STD 202, method 210: 260 °C, 20 s	+ 0.1
Thermal shock (96 resistors)	
MIL-STD 202, method 107: -65°C to +125°C, 25 cycles	-0.4
Humidity, 10 day (32 resistors)	
MIL-STD 202, method 103: 40°C, 95% relative humidity	+0.5
Elevated temperature storage (128 resistors)	
45°C, 10,000 h	+0.2
Life, operating, 26 mW (20.8 W/in.2, 640 resistors)	
MIL-STD 202, method 108, cycling 90 min power on,	
30 min off: 45°C, 10,000 h	+0.3

6. Stability of resistors in an ECL circuit is revealed by testing.



7. Planar resistors are incorporated in the same lead hole configuration used by discrete components in Cray Research's multilayer boards.

copper Layer 4 — Signal plane, 1-oz copper

E. Resistor characteristics: 25 Ω /sq sheet resistivity 0.050 in. by 0.025 in. resistor dimensions 50 Ω nominal value, 10% tolerance

32 resistors per board Test results are listed in Fig. 6. As can be seen, the resistors exhibited excellent electrical and mechanical stability.

Cray Research evaluation

Cray Research Inc., in an effort to improve product quality and reduce manufacturing costs, studied use of the planar resistor system. It was determined by cost analysis that by using planar resistor technology, Cray Research could realize an average cost savings per multilayer board equivalent to the cost of 140 discrete resistors, including labor and burden.

Cray chose to incorporate the planar resistors using the same lead hole configuration used by discrete components (Fig. 7). This was to enable them to implement the use of the planar resistor system quickly and at minimum cost. Only the 2.5 V layer needed

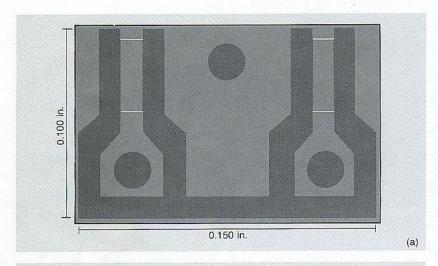
replotting.

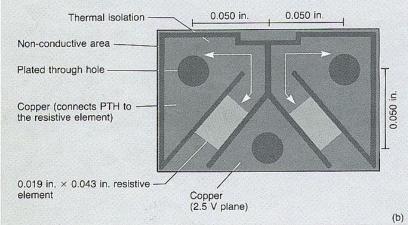
The initial resistor configuration was an 0.0165-in. wide by 0.045-in. long, 68-Ω value resistor. During heat stress testing, it was found that by changing the resistor design to incorporate a thermal isolation area between the resistor and the plated through hole, that the resistor stability could be increased (Fig. 8). This was accomplished by designing the resistive element on a bias between the plated through holes. Current designs have the resistive element right off the IC interconnect holes on 30-mil centers, freeing up the space once used for discrete resistors.

Results of the heat stress test, showing the stability improvement with the new design, are in Fig. 9. One hundred sixty-six resistors were subjected to six wave-soldering cycles, and a soldering iron was applied to each terminator for 10 seconds, with checking for resistor drift after each step. It was found that the average drift for the entire test was $+0.3 \Omega$ with a maximum drift of $+1 \Omega$.

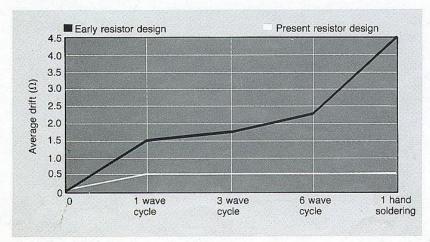
A 1,000 hour burn-in test was run while powering the resistors to 2.5 V (100 mW or 120 W/in.2 per resistor) in

Planar resistors boost PCB density.





8. Resistor design for Cray's multilayer boards was changed from the initial scheme (a) to incorporate a thermal isolation area between the resistor and plated through hole (b).



9. Heat stress testing shows the stability of Cray's initial and improved planar resistor designs.

a room-temperature environment. Average drift was $+0.21~\Omega$ and maximum drift was $+0.57~\Omega$.

A similar burn-in test was performed, except the ambient temperature was changed to 100°C. Most resistors exhibited significant resistance changes. Cross sections showed that the epoxy resin supporting the resistor had been burned away, indicating that the hot-spot temperature was well above the operating limit of the epoxyglass system.

Another test was run to determine at what operating temperature the resistors would start to drift. In this test 30 resistors were measured. Fifteen were operated at 1.3 V (28 mW or 34 W/in.² per resistor) and 15 at 2.5 V (100 mW or 120 W/in.² per resistor). The test started at 50°C; after every 100 hours the resistors were tested and the temperature elevated 10°C. The results indicated very little drift at lower temperatures. The 1.3 V test resistors were very stable up through 70°C.

Concurrently, Ohmega ran a 7,600-hour test per military standard 202, method 108 for power cycling. The resistors were powered at 125 mW (or 150 W/in.²) at 70°C. Average resistance drift was 2.5 percent.

Based on the various test results, Cray felt confident that the resistors would operate well beyond all normal voltages and temperatures. Tests were also performed on the resistors to check the susceptibility to transients. It was found that at 100 V, it took a pulse width of at least 6 ms to damage the resistors.

Cray Research's long-term reliability data is indicative of the high reliability the resistive material has exhibited. In over 12 years of field use, spanning many applications and users, there have been no reports of a resistor failure due to the resistive material.

Planar resistors incorporated into the internal plane of multilayer boards directly address the need for increasing circuit and package densities. Planar resistor technology has been shown to be a viable alternative to discrete and other resistor networks.