Keith Gurnett
and Tom Adams

Convergence of broadband with the wide variety of wireless channels, from Bluetooth through to WiMAX, makes the transmission towers and the base station key elements. The associated antenna and power amplifiers will play an important part in the continuing evolution of communication tools. This feature talks about some of the issues involved.

Considerations for GaN-Powered Base Stations

One of the key technology concerns of mobile telephone companies is the power amplifiers on the firm's mobile phone towers. Ideally, the mobile phone firms would like the power amplifiers to have high linearity, meaning that every channel being used has sharp edges. If channels have sharp edges, the amplifiers can transmit on much narrower channels and avoid Adjacent Channel Interference (ACI), and thereby make use of a much larger number of channels. Transmitting over more channels for the same cost is obviously desirable.

The mobile phone firms would also prefer – again, ideally – that the amplifiers be capable of operating at high power. Again, it's a matter of numbers: if a single amplifier can operate at higher power in a multicarrier system, you can serve the same number of customers with fewer amplifiers or towers.

At the moment, however, transmission towers use the silicon based RF LCMOS power transistors in their Power Amplifier Modules (PAMs). Some use of GaAs power devices in PAMs is also taking place, taking advantage of their superior frequency performance. The silicon devices are described as "medium power" devices whilst the GaAs devices are classed as "low power". GaN, a potential replacement chip material for use in PAMs, can operate at 100 to 150W. The latter is classed as "very high power" – meaning that the number of amplifiers needed, for a given transmitting output, will be significantly reduced by the GaN developments. In this article we examine some of the technical requirements that will be involved when the firms that supply transmission equipment move from silicon to GaN.

In addition to permitting higher power, GaN also handles linearity more efficiently than silicon does. Silicon runs at only 3–5V, but 0.5–1.0V of this is lost to forward voltage drop and saturation. GaN (as well as GaAs) run at 60V or more, but with the same 0.5–1.0V compromise, so the percentage loss is much smaller. The result: much sharper channel edges.

The makers of silicon chips are struggling to bring their specs up to the levels that mobile phone companies need, but they are running up against the physics of silicon, which limits what can be accomplished. Makers of conventional GaAs chips are gearing up to enter the fray, because GaN can often be produced in the same fab as GaAs. The day may not be far off when mobile phone companies can use a 100W GaN power amplifier to support many channels. Such an amplifier would replace the existing silicon power amplifiers.

GaN in Handsets, Too

The specifications and WiMAX protocols for using GaN chips in transmitting towers and in relay stations already exist; when GaN chips come onto the market, the standard will already be there to support them. WiMAX specifications are now being written to accommodate the use of GaN amplifiers in the mobile handset, to

enhance signal transmission from the handset back to the tower.

The advantages will be the same: higher power, greater linearity, and a greater number of channels. One major difference is that the number of mobile phones far outweighs the number of transmission towers.

GaN manufacturers understandably look forward to the day when GaN becomes the standard for handsets, and when every mobile phone manufacturer is incorporating GaN chips into their phones.

Packaging Diverse Materials

The WiMAX control system in the towers and in the handset will remain silicon-based, since its functions involve processing, management, routing and storage, but not signal transmission. When GaN arrives on board the mobile phone tower, it might seem natural to wrap both silicon and GaN in the smallest possible package – even stacking the chips, perhaps. But because of inherent differences in the two materials, such tight packaging will probably turn out to be impossible.

The primary difference is in the temperature at which each material operates. Silicon chips run at a maximum junction temperature of 180°C, while GaN operates most efficiently at 300°C. Packaging the two chips together would create terrific thermal problems. If both chips are run at 180°C to prevent damage to the silicon, the GaN chip will put out far less than the 100W it achieves at 300°C, and much of the advantage of using GaN in the first place would be lost. Mechanical and electrical separation of these two technologies complicates their interconnection in terms of the parasitic effects of inductance and capacitance. This could dramatically reduce the performance unless adequate decoupling and impedance matching are introduced.

The plastics currently used in the packaging of silicon devices have been developed and life-tested to accommodate only the 180°C silicon junction temperature; during assembly, the plastics will tolerate exposure to temperatures of 200–250°C for brief periods. GaN power devices, on the other hand, need to be packaged in ceramic if the junction temperature and higher power capability is to be fully utilised.

Since the GaN device in the power amplifier will be running at 100W, the ceramic package needs

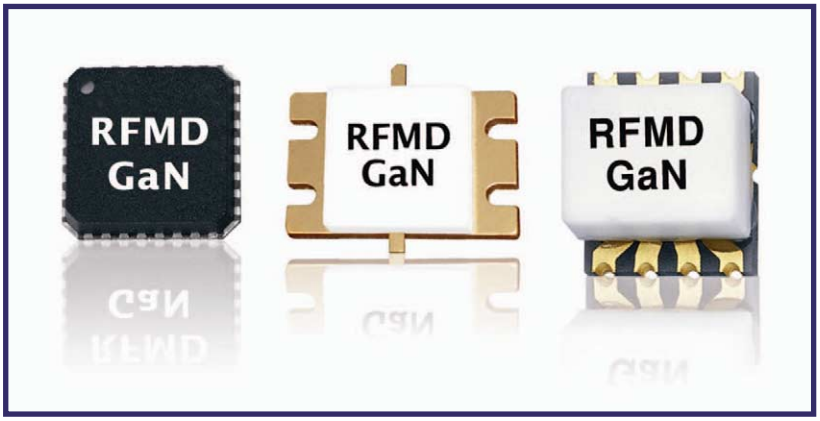

Figure 1. RFMD's GaN range of packages, showing the bolt-down version in the centre.

to be attached to a heat-sink, whose temperature should not exceed 80–100°C. This demands very efficient thermal extraction of heat from sink to ambient, and for this level of efficiency an air or liquid cooling system will be needed. The ceramic GaN package will have bolt-down facilities to ensure intimate thermal contact with the heat-sink. This type of package is the central package shown in **Figure 1**.

Decoupling and Impedance Matching

The interconnection from the silicon control system (complex ICs involving processor and control elements) to the GaN power amplifier element will probably originate from a high pin count device, probably in a BGA-type format. In order to connect to and pass through the pin-out system, the printed circuit board will require small geometry of an HDI (High Density Interconnect) nature. In order to achieve these dimensions thinly clad copper material is invariably used in board manufacture. (Thicker copper would be unacceptably undercut during the longer etch process that it would need.) For some boards the additive process is employed where plating up through a mask is used to create the pattern of fine lines and pitches.

This thin trace in conjunction with small gap and track dimensions creates a conductor of small cross-sectional area, and will produce a resistive line to the output device. Good decoupling will be needed at the device terminals in order to support the high frequency current demands from the output PAs. Capacitors will be needed that have very low inductive lead-outs from plate to terminal. Values up to 100µF are required within the total power system. These capacitors are normally relatively large and need to be

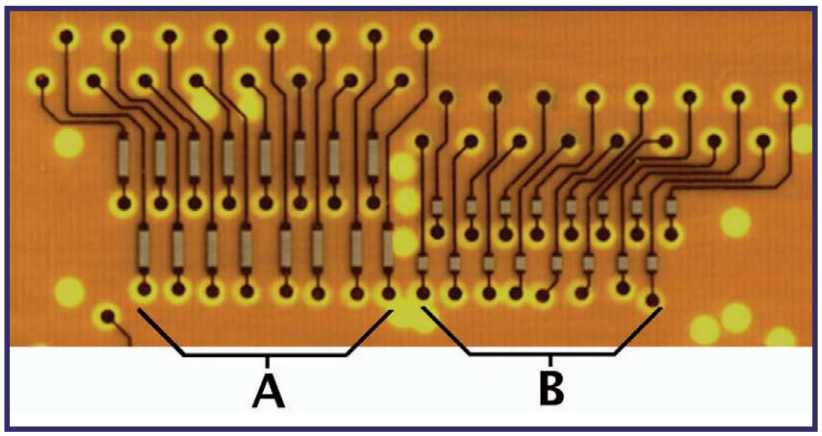

Figure 2. A layer of 32 resistors for embedding using OhmegaPly™ material. (A) shows two banks of eight resistors measuring 4.0 × 1.0 mm of 10 ohms per square material, giving 40 ohm for each resistor. (B) shows two banks of eight resistors measuring 1.5 × 1.0 mm of 10 ohms per square material, giving 15 ohms per resistor.

mounted next to the power package. Judicious placing of smaller values (up to 1000pf) can alleviate the use of such high values elsewhere, as long as an evenly distributed power system has been designed into the board.

Since HDI will be needed, the trace-to-trace cross coupling is high, and significant inductive and capacitive elements will be formed by the interconnect conductor system. The matching impedance element levels required are of the order of up to 50mH and 4pF, dependant on the input/output impedances of the devices. The interconnect contribution to these values, in terms of parasitics, can be significant if long multilayer and densely placed traces are employed. In both cases placing these terminating/decoupling components physically at the terminals of the device to be decoupled or terminated is extremely important. It is also imperative to take into account the circuit parasitics. Getting physically close to the actual devices is best achieved by embedding these passive components next to the device they are compensating within the interconnect system.

Embedding

Whilst there are various ways to embed components into the interconnect system there are two major issues that determine the method to be used: (1) component availability in terms of size; and (2) the combined cost of the component and method used to embed. The combined cost may, of course, be mitigated by the number of additional channels gained by the use of GaN.

Components

There are some manufacturers of small value inductor and capacitor components suitable for embedding. In fact if the interconnect core is relatively thick, standard SMT components can be used under certain conditions. Some of the lower values of SMT chip resistors are less the 70 microns in height. Small inductor values can be achieved by creating coils in the traces. Capacitor values can be manufactured by the use of film systems such as Faradflex .The dominant problem component is the decoupling capacitors. Creating large values of C is difficult in terms of unit area, even in FaradFlex, and multiple use of small values in banks is often the solution.

A similar technique for embedded resistors has been around for some time. The OhmegaPly system uses a resistive coated laminate that can be patterned to form resistors. The limitation to this technique is that only one resistivity per layer can be used. Hence the range of resistors per layer is only about three decades. A patterned resistive layer of a multilayer circuit board is shown in **Figure 2**.

Embedding Techniques

Cutting apertures in one of the interconnect layers and placing thin passives within the cavity enables placement close to the active device. The thickness of the layer used has to be sufficient to allow the embedding of the passive without surface bowing after laminating. This layer could be purely Resin Clad Copper (RCC) and the component will automatically be embedded during lamination without the need to cut apertures. If woven glass fibre is used the glass mat has to be cut in order to avoid surface distortion.

With prepared films, both resistive and capacitive, the components are defined using lithographic techniques and sited as near to the active device as possible. Resistive ranges are limited by the resistivity of the material. As there can only be one resistivity per layer, variations of resistor values over more than three decades of value tend to be difficult to manufacture; *i.e.* one square through to 30 squares in terms of length/width ratio is practical and results in reasonable yields. Any greater ratio is difficult to produce with any degree of reasonable tolerance of end value. Trimming using abrading or laser techniques could adjust these values into tighter tolerances, but trimming is an added cost.