PASSIVE DEVICES
BURIED RESISTORS

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INTRODUCTION

Typically resistors are second only to capacitors in the quantity required per card using a great deal of the available surface real estate. Cards or printed wired boards (PWB) have more functions per card today than those of ten years ago, resulting in more components. More functions mean more possibilities of signal degradation because of cross talk or reflections. Resistors are used to condition the signal lines for the best possible quality by reducing overshoot and undershoot caused by reflections found in high speed signals. From a design point of view all signals need to be as clean as possible. Bus speeds are increasing rapidly where 100 MHz or more will not be uncommon. Bus width has grown in the last decade from 8 bit, to 16 bit, 32 bit and now 64 bit. The speed increase makes reflection reduction even more critical, and the wider bus increases the number of resistors needed to reduce reflection. Increasing the number of passive components means that the cost of the assembly increases while the throughput decreases. As concluded in an article appearing in Circuits Assembly, "Ultimately a new, low-cost paradigm for passives will be required."[1]

A win-win situation is where development can have as many resistors as required without space constraints or trade-offs, and manufacturing can increase throughput. One possible strategy is to embed the passives where possible in the raw card. Ohmega Technologies Inc. has developed a process where resistors can be buried in the raw card. The technology has been used for over twenty two years in companies such as Cray Research, Unisys and others.

A study completed at IBM PC Co. Austin, will determine the feasibility and effects the assembly process has on buried resistors. Some of the driving factors behind the study follows:

- Improved EMC
- Improved Signal Quality
- Greater throughput capacity in assembly manufacturing
- Higher yields in assembly manufacturing
- More card surface area available
- Avoid use of 402's
- Reduce the required number of test points
- Simplified test fixtures/Improve test times
- Reduced inventory on parts
- Overall quality improvement

The concept applied in the study takes a range of surface resistors between the values of 10Ω to 10KΩ with tolerances greater than 5% and embeds them in the PWB. If you analyze the value of resistors in the bill of material for most products, more than 75% of the resistors will meet the previously stated criteria. Typically this will remove between 10 to 15 part numbers from the bill of material. The resistors are removed from the bill of material and replaced by being buried in a PWB using the Ohmega-Ply® thin film resistive material. Is the Ohmega-Ply® technology a viable strategic alternative to surface mount technology (SMT) resistors? Does the strategic advantage out weigh the material cost? Some of the same arguments used when making the transition from pin through hole (PTH) technology to SMT is applied to embedding passives.

The requirement for partnerships is one of the major factors keeping Ohmega-Ply® relatively unknown in the computer industry for the past twenty two years. To implement embedded resistors takes joint partnerships with development, panel manufacturing and assembly manufacturing. IBM is in the unique position of having all of these areas within one corporation to fully exploit the advantages of a strategic technology such as Ohmega-Ply®.

PLAN OF ACTION

A partnership between IBM Austin ECAT and IBM Endicott was formed to determine if the Ohmega-Ply® technology is a viable strategic alternative to SMT resistors. IBM Austin ECAT would provide the test vehicle (TV) development and assembly manufacturing requirement and IBM Endicott would provide the panel process manufacturing qualification requirement. In parallel, the data would also be given to an IBM qualified vendor working with IBM Austin panel manufacturing. The vendor cards would then go through qualification for assembly manufacturing in IBM Austin ECAT. IBM Endicott would qualify the technology using the cards produced through their process. The next phase would involve an actual product. **Note:** IBM Austin panel and IBM Endicott have since determined not to pursue buried passives until product loading is committed.

All tasks in IBM Austin were accomplished without a budget. The various departments within IBM ECAT Austin recognized the potential for embedding passives and were willing to work as a team to reach a decision point. ACD (Automated Circuit Design), a local vendor in Texas agreed to work with IBM, based on their past experience, to produce a test vehicle and actual product. Chuck Michie, Vice President of ACD, was instrumental in the project.

Table 1. PLAN OF ACTION

TEST	Phase 1: Test Vehicle	Phase 2: Product
DSDP Assembly	15 cards	Mobile
HYBRID Assembly	15 cards	Power PC
ATC 50 cycles, 0-100°C, 20 min dwells	30 cards	20 cards
Torque	15 cards mix	None
Ship/Shock & Vibration	15 cards mix	
EMC	2 cards	2 cards
Signal Quality	3 cards	2 cards
Guard Band	None	3 cards
Pressure Cooker		
Thermal Cycle Test		
TH & B	No Bias	2 cards
Solder Shock	1 card	1 card
I/O Characterization	1 card	
Thermal Aging	6 cards	
ATC	6 cards	
Power Cycling	6 cards	
T/H	6 cards	
Torque/Wet Thermal Shock	6 cards	

Test Strategy

The following test strategy was agreed to by Austin ECAT manufacturing based on initial plan from IBM Endicott Panel manufacturing.

1. The maximum resistor tolerance = 20% of the required value.

   Key components:

   a. Raw material tolerance

   b. Effects of raw card processing

2. Reliability criteria = maximum 3% delta from T0 value

   Key components:

   a. Effects of component assembly/rework processing

   b. Life conditioning - Bias with Temperature Aging, Thermal Aging, Temperature/Humidity, Torque-Wet Thermal Shock

3. The TV will have resistors made from 25Ω/□ and 100Ω/□ sheet resistive material.

4. The resistor values of general interest are:

Table 2. TV Resistor Values	
VALUE	QTY
25 Ω/□material	
10 Ω	40
100 Ω	44
1K Ω	60
100 Ω/□material	
33 Ω	30
1K Ω	30
10K Ω	40
284/card * 30 = 8520 total resistors	

5. The resistor values monitored during reliability testing are:

Table 3. Resistor Delta	
VALUE	3% Max Δ
25 Ω/□material	
10 Ω	0.3
100 Ω	3.0
1K Ω	30.0
100 Ω/□material	
33 Ω	0.9
1K Ω	30.0
10K Ω	300

Note: Resistors of other values will be on the TV and will be tested at the core and composite raw card level.

6. Conditions

   a. The power rating = 1/16 and 1/8 watt

   b. The maximum applied voltage = 5 volts

7. The resistor of interest is series terminating and pull-up.

8. Use the TV designed for Endicott testing.

9. Each resistor net will be accessed by a 2x12 100 mil stick header.

10. The technical concerns are:

    a. To build resistors of different values to given tolerance.

    b. To effectively test the resistors at the core/raw card (The composite level resistor rework process will be the already qualified standard delete and wire add process.)

    c. Raw and assembled card processing effects because of chemical, thermal, or mechanical factors (delamination, etc.)

    d. Characterize resistor stability due to aging (reliability)

e. Thermal Characterization (Heat rise, Power dissipation)

f. Characterize the resistors based on:

1) Sheet resistance types (25 or 100Ω/□)

2) Signal and power plane termination

3) Resistor Patterns (Bar, Serpentine, Circular)

4) Orientation of resistor

5) Resistor width (Establish tolerance design window)

11. Test vehicle design strategies

Place both sheet resistance on same TV. One set of signal and power planes dedicated to a study of 25Ω/□ material; the other set to 100Ω/□ material. Build resistors of values representative of the application.

- Advantage = 1 TV design covers technical concerns.
- Disadvantage = Stress test logistics (cabling)

12. Test Strategy

a. T0 Characterization - 1 card/test cell (sheet resistance)

b. Test Specification

1) 871889 - Raw Carrier/Assembly Reliability Testing

2) 895049 - Fixed and Film Resistor Requirements

c. Stress Testing (Note 1) - 6 cards/test/critical variable (Note 2)

1) Thermal Aging (Performance stability)

2) ATC (Material stability)

3) Power cycling

4) T/H (Material stability)

5) Torque/Wet Thermal Shock (Mechanical stability)

6) Corrosive Gas (Note 3) (MFG1, MFG2)

Notes:

1) Test hardware will be subjected to a simulated component assembly operation for pre-conditioning (Operations TBD)

2) Critical variables

a) Sheet resistance types (25 or 100Ω/□)

b) Signal/power plane termination (Thermal characteristics)

c) Resistor Patterns (Bar, Serpentine, Circular)

d) Orientation of resistors

3) This test along with basic thermal characterization can be tested at the core level, prior to T2 testing.

Assembly Process

The IBM Austin ECAT team agreed to the most stringent assembly process that would stress the test vehicle. There were a total of 30 cards available. Half of the cards were to go through the Double Side Double Pass (DSDP) process and half through the HYBRID process. The DSDP process involves going through the infra red (IR) convection oven twice. The HYBRID process involves going through the IR for topside components and then the solderwave for backside components. 3 cards, in each group, had the pin grid array (PGA) socket reworked. All cards had the Ball Grid Array (BGA) reworked twice, with 4 cards, in each group, reworked 3 times.

Stress

IBM Austin ECAT agreed to stress the cards by performing ATC, Torque, and Ship/Shock & Vibration on all 30 cards. All 30 cards were put in to the chambers for ATC testing. The local Austin reliability team agreed that 50 cycles , 0 - 100 °C, with twenty minute dwells would be sufficient for ECAT assembly manufacturing. A mix of the DSDP and HYBRID cards were then used for the Torque testing and also for the Ship/Shock & Vibration.

EMC & Signal Quality

The test vehicle was designed with 74ABT16245's and an oscillator footprint so that EMC testing could be done at various frequencies. Half of the signals from each device were dual footprinted so that either buried or SMT resistors could be placed on the card for base line comparisons. Matched line lengths were incorporated for testing signal quality. The line lengths varied from 6 inches to 8 inches with 2 of the lines running in parallel.

Product Verification

The cards had all the resistors measured in IBM Austin ECAT QTAT using the Takaya Fixtureless Tester Model APT 2200N tester. Since the APT 2200N Model did not have a specification for the resistor measurement accuracy, one card was selected and tested three consecutive times. The results showed there was less than 1% change in the three measurements. However, there was erroneous data resulting from a probe slipping off or missing the test point. If the test result was attributed to error from the tester then it was discarded. The configuration of the design also impacted the data. Many of the resistors could not be isolated for an accurate measurement on the raw card because of parallel nets. Subsequently after each phase the cards had the resistors measured again, for a total of 5 data sets. The criteria for the assembly process and stress testing was a resistor value change no more than 3%.

TECHNICAL

Material

Ohmega-Ply® is a thin film metal alloy that is laminated to a dielectric material and subtractive processed to produce planar resistors. The lower layer is electrically resistive material, Nickel Phosphorous (NiP). The upper layer is Copper (Cu). Material is available for production at 25 Ω / □ (16 μ inches) and 100 Ω / □ (4 μ inches).

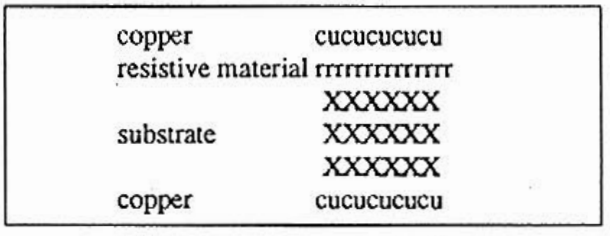


Figure 1. Laminate with resisteive material

Bruce Mahler of Ohmega Technologies Inc., has written an excellent paper on the process required for planar resistor technology.[2] Refer to the article for detailed information of the resistor fabrication process.

Geometry

There are two types of geometry for designing resistors: bar and serpentine. A third option is the circular type which is still experimental and has not been found to be practical now. A bar resistor is formed by combining squares using the formula:[3] $R = Rs\ (L/W)$. The smallest bar resistor possible is 1/3 of the resistive material value or a partial square. For example, on 100Ω/□ 1/3 of 100 is 33.3 or a 33Ω resistor. The serpentine resistor must take the corner squares into account. "Due to the change in current density at right-angle path, the effective number of squares is 0.559, which is commonly used in resistor design."[3] The serpentine resistor is calculated using the formula:[3]

$$R = Rs \times (Wsq + (Csq \times 0.559))$$

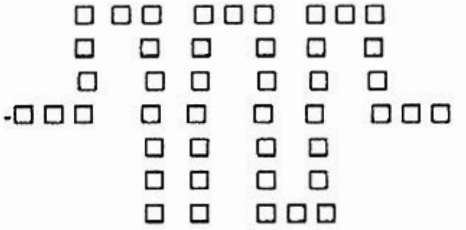
- Rs => sheet resistivity Ω / □
- L => length
- W => width
- Wsq => number of whole squares
- Csq => number of corner squares

Bar example: 25 Ω / □ to make a 100 Ω resistor requires 4 squares.

□□□□

The L and W are the physical designer's choice. The TV used 10mil x 40mil. From the data collected on the TV larger dimensions are required for bar type resistors. Alcatel Bell and INTEC found that underetching affects the resistive value. "It is clear that, for a given variability of the underetching, the effect on the resistor tolerance is larger for resistors with small dimensions than for resistors with large dimensions."[4]

Serpentine example: 25 Ω / □ to make a 1K Ω resistor requires 33.3 squares and 12 corners.



Test Vehicle

Description

The test vehicle (TV) was designed using both the 25Ω/□ and 100 Ω/□ material. The 25 Ω material was on the signal layer and the 100 Ω material was on the power plane. Resistor values of 10 Ω, 100 Ω, and 1KΩ were on the 25 Ω layer. Resistor values of 33 Ω, 1KΩ, and 10K Ω were on the 100 Ω layer. Values were chosen to bracket the expected range of resistors for the value of material used to keep the size of the buried resistor close to an 0805 SMT package. The lower resistor restriction is set by the material value used at 1/3 of the material value.

Sections of the card were designed to test EMC, signal quality, manufacturing rework and panel process. The EMC and signal quality section were designed using 74ABT16245's, 2 for each layer for a total of 4 devices. The inputs were tied to +5V through a buried resistor. The outputs passed through series resistors with pull-ups going to 2x12 100 mil connectors. Half of the outputs also had SMT pads in parallel with the series resistors, and the other half of the outputs were tied to ground. Outputs to the connectors varied from 6 inches to 8 inches with two of the lines running in parallel. A generic oscillator footprint was included to vary the speed of the active devices. Some of the 10 Ω and 33 Ω resistors were placed under a PGA socket to test the manufacturing rework impact. A BGA footprint was placed on the card to test the effect extreme heat had on surrounding resistors. A section on each layer has resistors with 10 squares forming a bar resistor. The width was varied from 20 mils, 10 mils, 9 mils, 8 mils, 7 mils, 5 mils and 4 mils, each width had 5 resistors. The plan is to compare exactly the material differences and process impacts for the various widths. The value for 25 Ω / □ was 250 Ω and the value for 100 Ω / □ was 1K Ω.

COST

Early in the study it was determined that direct cost savings was not the motivating factor. Resistors are buried when the signal speeds are 75 MHz or greater or driven by PWB real estate. Based on the volume pricing from Ohmega Technology Inc. and the added process cost, generally the additional can be anywhere from $2/card to $33/card, depending on the size of the PWB. There are instances where the card size may be reduced because of embedding resistors allowing more cards per panel and therefore reducing the PWB costs. A generic cost analysis is available from Ohmega Technology.[5] The cost factors are based on industry standards and does not necessarily represent cost found within IBM.

Breakeven Point

Cost benefits are noted when over 100,000 ft² per year of material is used. Generally, the additional cost for using over 100,000 ft² per year was around $6 per card. Cost advantage occurs when the following conditions are met:

- Resistor density exceeds a minimum of 6 to 10 resistors per square inch.
- More than 75% of the total resistors can be removed from the surface.
- Maximum raw card panel is utilized or improved.
- 100,000 ft²/year + is used of the Ohmega-Ply ® material

RESULTS

This section describes the results from the test strategy that was actually accomplished. IBM Austin ECAT furnished all the test results.

Assembly Process

Of the thirty cards assembled and tested, the data did not indicate any significant impact on the resistor value from the assembly process. The resistor values changed less than 3% overall and generally less than 1%. The rework of the PGA and BGA also did not impact the resistor values. Data results are shown in the appendix.

Stress

Of the thirty cards that underwent stress, the test data did not indicate any change in resistor value.

The following test were performed on the 30 buried resistor cards.

1. Thermal cycle

All 30 cards were stressed for 50 cycles with 20 minute dwells from 0 to 100 degrees C.

2. Thermal Shock T/S

   A total of 15 hybrid and DSDP cards were placed in T/S chamber for 5 cycles with 30 minute dwells from -40 to 65 degrees C.

3. Vibration Test

   The same 15 cards from T/S were used for vibration. IBM standard V5N test was used for vibration.

4. Torque Test

   The remaining 15 cards were used for torque test. Each card was torqued at 100 in. lbs. and 6.6 degrees for 25 cycles.

The following were not accomplished as stated in the test strategy:

- Bias with temperature aging
- Corrosive Gas testing
- Circular resistors testing

EMC & Signal Quality

At initial power the 74ABT16245's were extremely hot, and the power supply showed approximately 4.5A. Desoldering the output pins tied to ground decreased the current to 2A.

Signal Quality testing was done using a HP6500 Digital Oscilloscope. A high Z-pot was used to open the buried resistors. The high Z pot consisted of applying high voltage low current across the resistor. Bar resistors less than 20 mil wide would open at 20 volts. None of the serpentine resistors were opened because of the limitation of the power supply. As expected, no damage was noted to the 74ABT16245. At 50 MHz no noticeable signal improvement or degradation was noted between buried or discrete resistors. At 143 MHz the signals again showed no change between buried or discrete resistors.

EMC testing is not complete at this time for the TV. A product is in process of being assembled and tested. A bench mark is already established with the original design.

Power Rating

Power dissipation is a concern for design engineers, and for most applications 1/8 W is sufficient. To verify the statements made by Ohmega Technology regarding the recommended power dissipation a TV was sent to them. James Tso of Ohmega Technology did a short-term load test for the resistors on both the 25Ω layer and the 100Ω layer. The power applied to the resistors was increased every two minutes until the resistors became unstable and opened. Every resistor exceeded the expected power dissipation except for the 100 mil wide resistors. The calculated value for the 100 mil wide resistors were not met. The equation used to predict the power dissipation is general and based on the assumption the material would dissipate 100 W/in^2. Obviously, there is some anomaly that occurs as indicated by the 100 mil wide resistors which may be attributed to the 100 W/in^2 assumption used in the equation.

Note: Refer to the appendix for power rating data prepared by James Tso of Ohmega Technology Inc.

$$P\ \text{Watts} = (\text{Area in}^2) * (100\ \text{Watts/in}^2)$$

Refer to the material specifications for specific details. The next table gives a summary of the data.

Geometry

Logic designers and PWB manufacturers are at odds in the geometry of the ideal resistor. Logic designers want the smallest possible dimensions (4 mil wide) while the PWB manufacturers want the largest possible dimensions (20 mil wide). 10 mil wide was chosen as a compromise for a starting point and the majority of the resistors were 10 mil wide.

The TV partial square resistors were 30 mil x 10 mil. The PWB manufacture was instructed not to change any of the dimensions during the process. Results were as expected. Bar and partial square resistors geometries added to the result of the bell curve being offset from the expected value. Serpentine resistors also experienced a shift in the bell curve. The partial square resistors would be expected to have better tolerance if they were designed with larger widths such as 39 mils or 42 mils, or any even multiple of 3. (This was proven true in a later design.)

Table 4. POWER CALCULATION & MEASUREMENT

Resistor (ohms)	Type	Ω/□	Width (mils)	Length (mils)	Expected (W)	Actual (W)
10	Partial	25	30	12	.04	.236
100	Bar	25	15	60	.09	.349
100	Bar	25	10	40	.04	.156
250	Bar	25	20	200	.4	1.442
250	Bar	25	10	100	.1	.384
250	Bar	25	5	10	.03	.192
4.7K	Serp	25	8		1.36	3.013
4.7K	Serp	25	10		2.12	5.659
33	Partial	100	30	10	.03	.145
422	Bar	100	100	422	4.2	3.024
1000	Bar	100	5	50	.03	.139
1000	Bar	100	10	100	.1	429
1000	Bar	100	20	200	.4	.982
1200	Bar	100	100	1200	12	6.912
10K	Serp	100	5		.28	.752
10K	Serp	100	10		1.13	1.474
47K	Serp	100	10		44.89	4.573

The histograms shown in the appendix include all the targeted resistors. Since no distinction was made in the naming conventions for the 100Ω or 1KΩ resistors the data is shown in one chart. The partial square resistor, 10Ω ,indicates the mean at 12Ω. The 33Ω resistors were fairly consistently on target. The 100Ω resistor has distinctive clusters showing the parallel nets. The isolated resistors were on target. The 250Ω resistors were only on the 25Ω/□ layer and isolated from all other circuits. The width stepped from 20 mil, 10 mil to 4 mil, which attributes to the spread. The 1KΩ resistors were on both layers with mixed geometry, bar and serpentine. Both instances showed resistors to be on target. The 10KΩ resistors were only on the 100Ω/□ layer and essentially on target.

Serpentine resistors require an additional square for misregistration during the etch process. Most serpentine resistor applications would not require more than 20% tolerance and all the serpentine resistors fell within that range. The tolerance difference between the 5 mil, 8 mil, and 10 mil serpentine was less than 1% based on the TV sample size. Also, the 5 mil serpentine was 1/2 the size of a 10 mil serpentine making the 5 mil serpentine a logical choice for serpentine designs.

CONCERNS

During the study six concerns surfaced. The first three will be resolved with wide spread applications.

- Cost
- Material consistency
- Single source material supplier
- Engineering changes (EC)
- Resistor tolerance
- Power rating

The question regarding EC rework on the PWB is best addressed during the design phase using signal analysis. Signal analysis or simulation is

recommended to determine the correct resistor value for series terminators or pull-ups/downs. Happy Holden of Hewlett Packard strongly recommends signal analysis for successful implementation and to avoid EC's. Currently resistor tolerance is board fabricator dependent. Through experience a library can be built with the best possible dimensions for a wide variety of process capabilities and flatten the board fabricator dependency. The power rating is not an exact calculation and for series terminating or pull-up/down resistor applications the general equation will be adequate. Many of the concerns are the same as when the transition from PTH to SMT was made and will be addressed in a similar manner as the process matures.

CONCLUSION

The data from the TV study indicated the buried resistor technology is a viable strategic alternative to SMT resistors. There was no indication the manufacturing assembly process affected the buried resistors. However, the six areas of concern need to be addressed before large scale implementation is initiated.

The cost analysis presented by Ohmega Technologies Inc. clearly shows the cost effectiveness point exists around 2 to 4 resistors per square inch. Using industry standards for parts cost and PWB cost, the breakeven point is around 6 to 10 resistors per square inch. On a product by product basis the cost will not be the reason for using buried resistors, unless the material use exceeds 100,000 ft^2 or the board size is reduced to allow more cards per panel. An accurate analysis can only occur when all products are considered. When a mixture of products meets all the requirements for using buried resistance then there is a high probability that a cost advantage exists. Each company must determine the strategic advantage over the material cost based on their own strategic plan.

The cost advantage was not conclusive based on available IBM data. All the factors are there to indicate that IBM would realize huge savings if this process was applied across all product lines.

Next generation computers will have challenges not even considered today. Like an onion, the concerns and issues around buried components need to be unlayered to get to the heart. To keep pace with chip design technology the PWB technology must push the envelope of the perceived process concepts. Tomorrow's technology is being designed today and has higher requirements. In five to ten years, buried components will be as common as SMT devices are today.

APPENDIX A. TEAM

Without the assistance, support and belief by the people listed below this project would not have been possible. Each person contributed their expertise to the success of the study.

IBM Austin

Cynthia L. Martin	Project Lead
Derrel Webb	Cost Analysis
Rick Mitchell	Physical Designer
Wayne Collins	Reliability
Leo Anderson	Reliability
E.Wayne Hayes	Stress Lab Engineer
Bill Carreon	Stress Lab
Ron Kalin	Stress Lab
Atruo Urias	QTAT Engineer
Tim Lippe	Assembly Process Engineer
Ron Leadbeater	Cost Models
Eric Hills	Austin Panel
Karl Hoebener	Austin Panel
Betty Whalen	Austin Panel

IBM Endicott

John Lauffer	Project Lead
Gary Kratochvil	Reliability Lead
Joe Resavy	Physical Designer

Vendors

Bruce Mahler	Ohmega Techonolgy Inc.
Chuck Michie	Automated Circuit Design

APPENDIX B. DATA

Test Vehicle Cross Section

Figure 2. Test Vehicle Cross Section

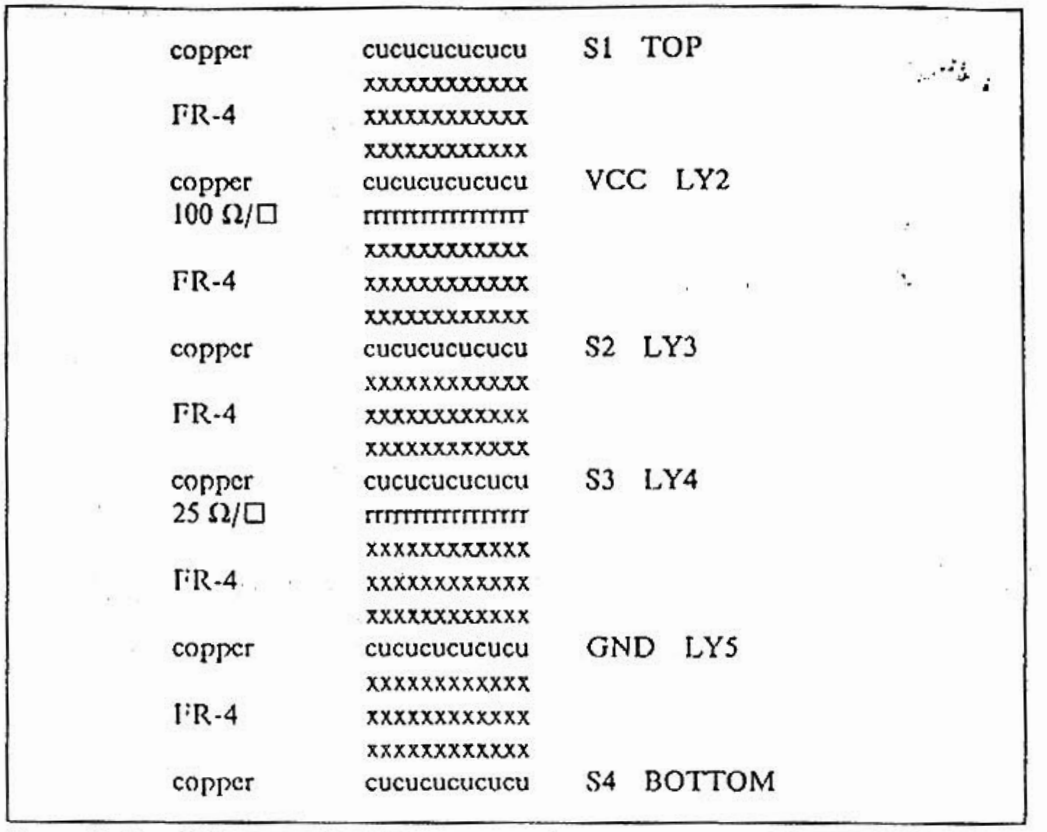
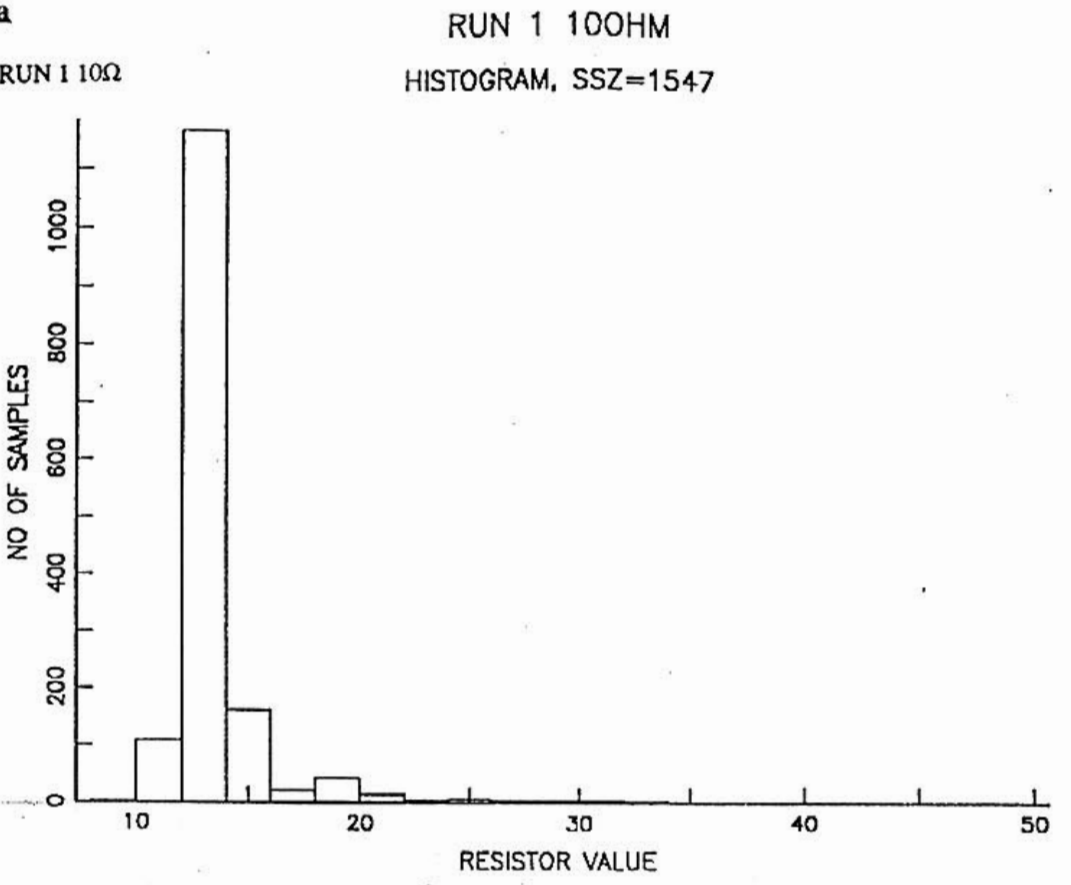


Figure 2. Test Vehicle Cross Section

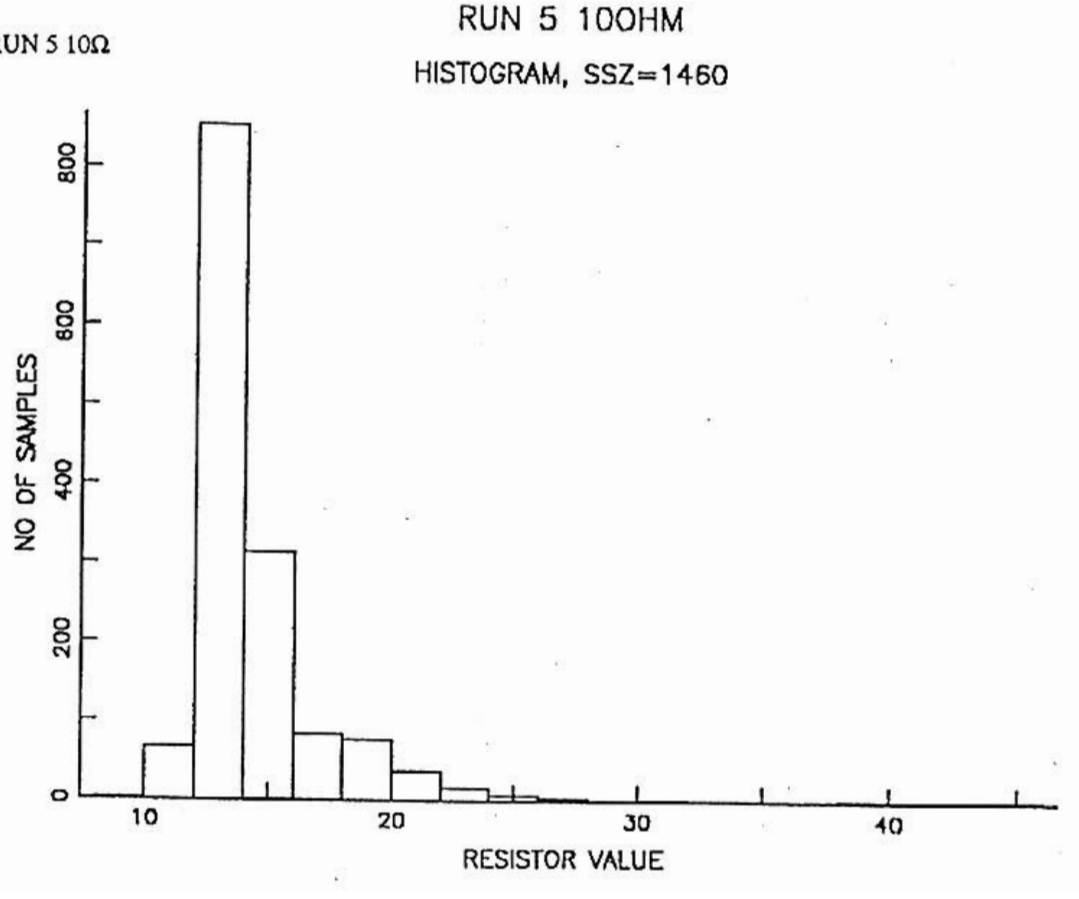
Test Data

Figure 3. RUN 1 10Ω



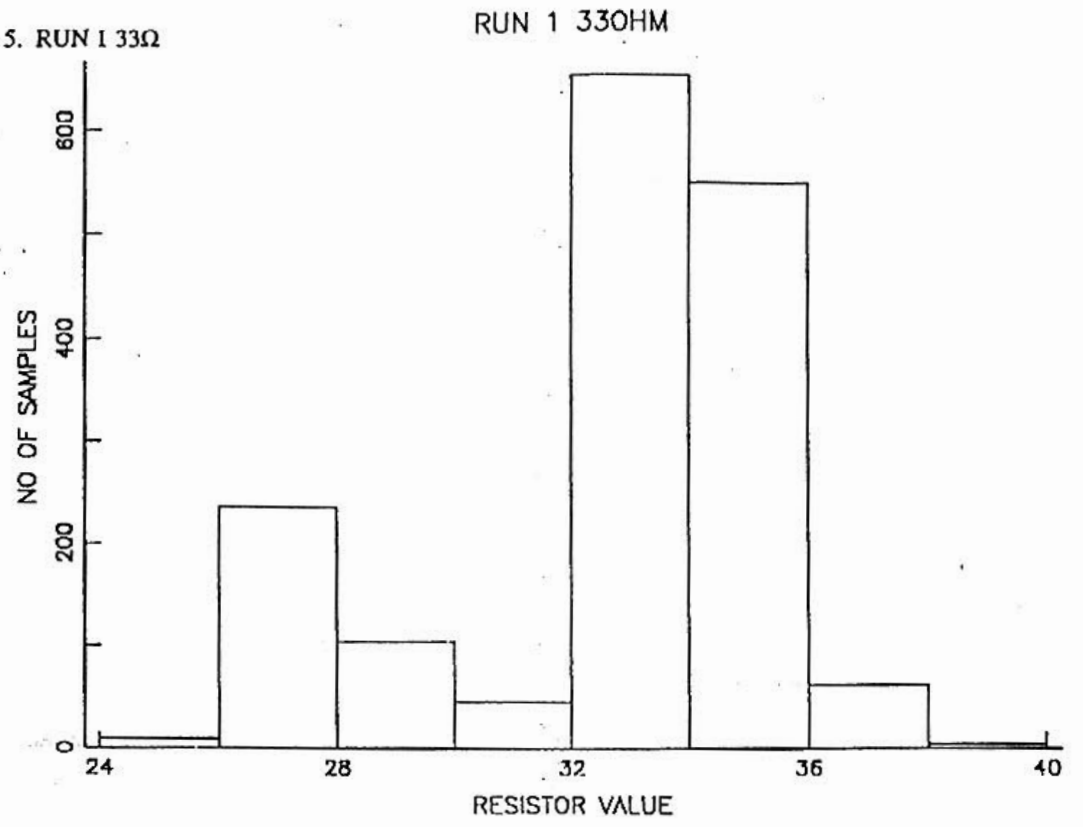
Test Data

Figure 4. RUN 5 10Ω



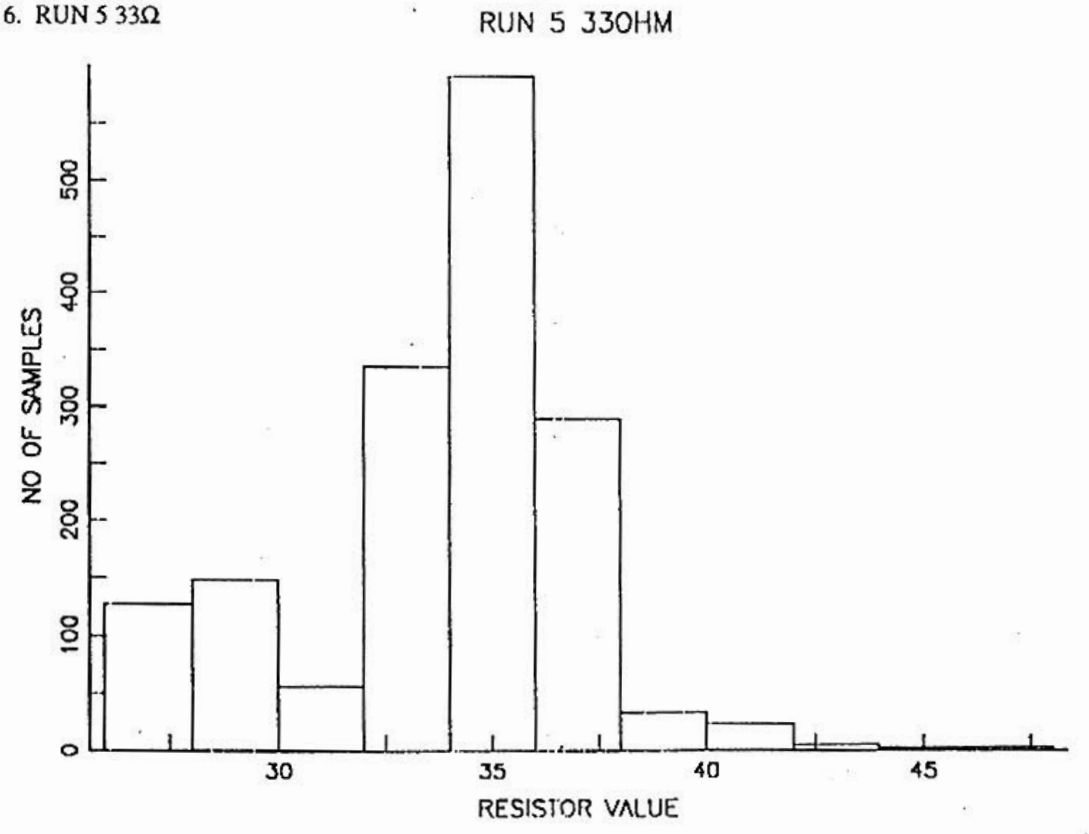
Test Data

Figure 5. RUN 1 33Ω



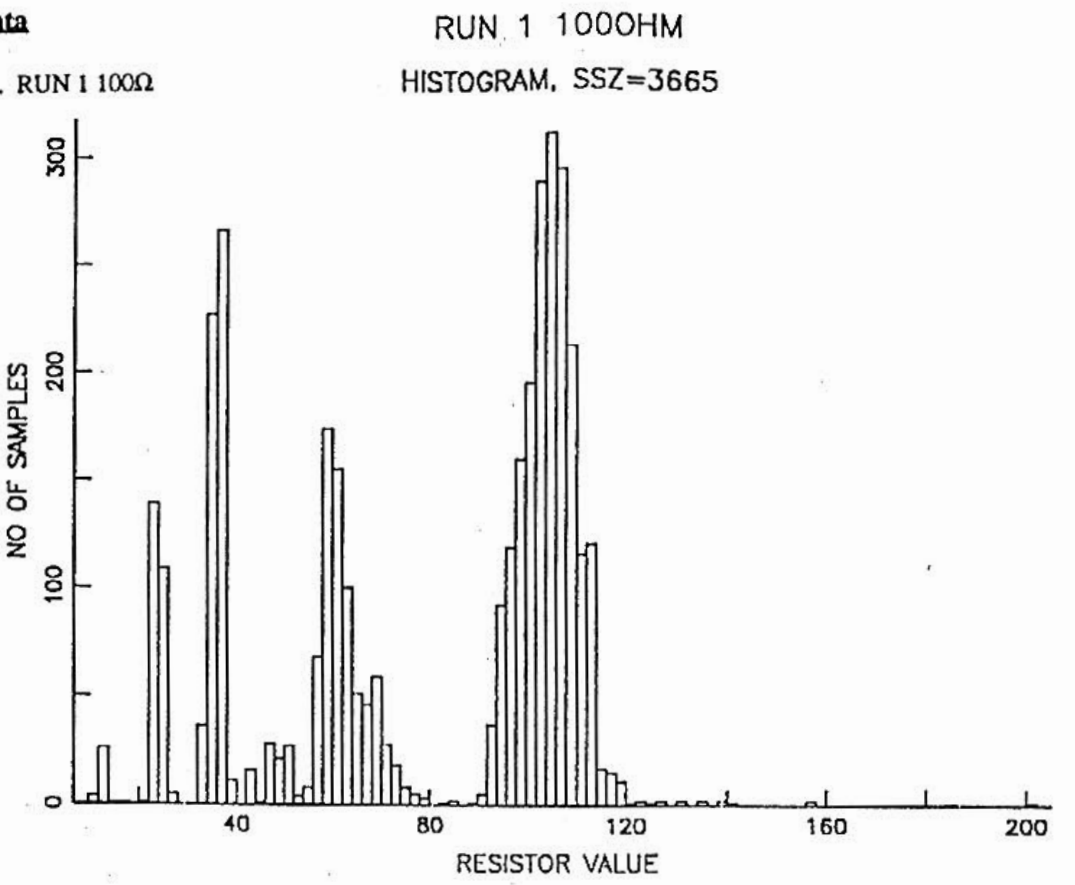
Test Data

Figure 6. RUN 5 33Ω



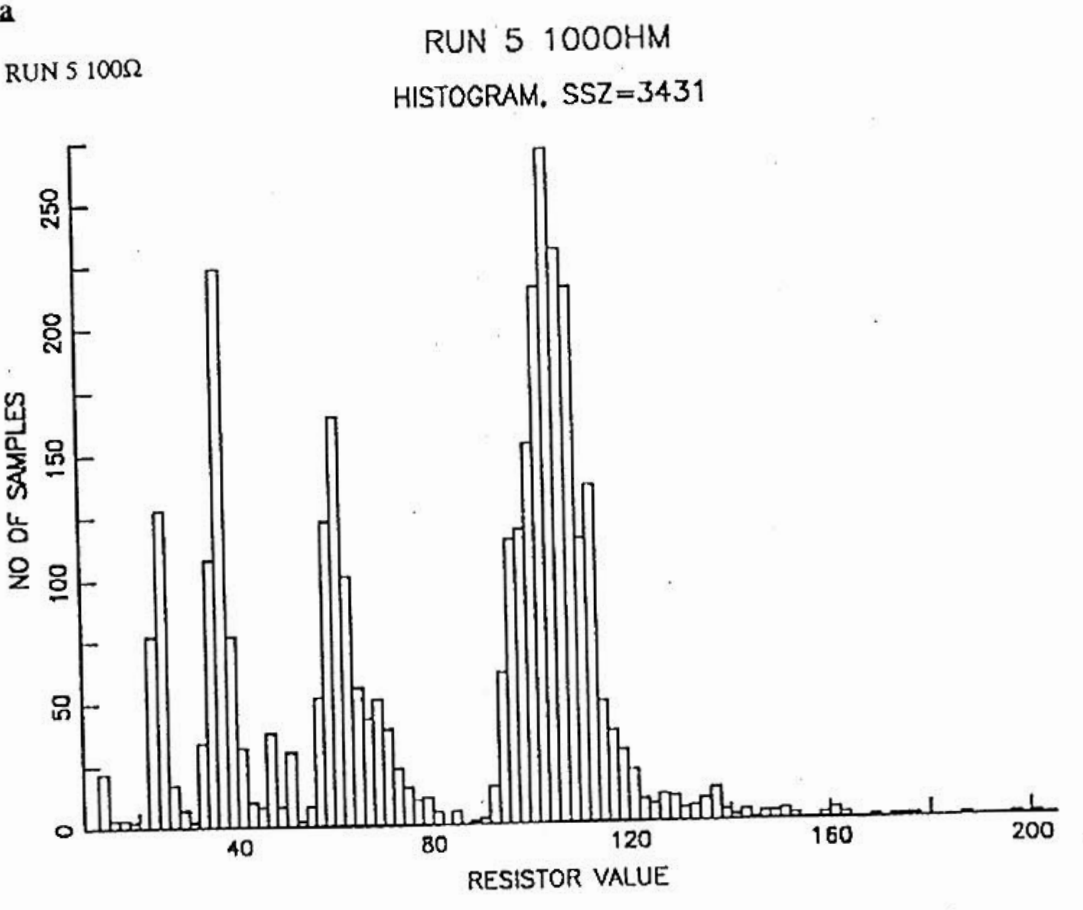
Test Data

Figure 7. RUN 1 100Ω



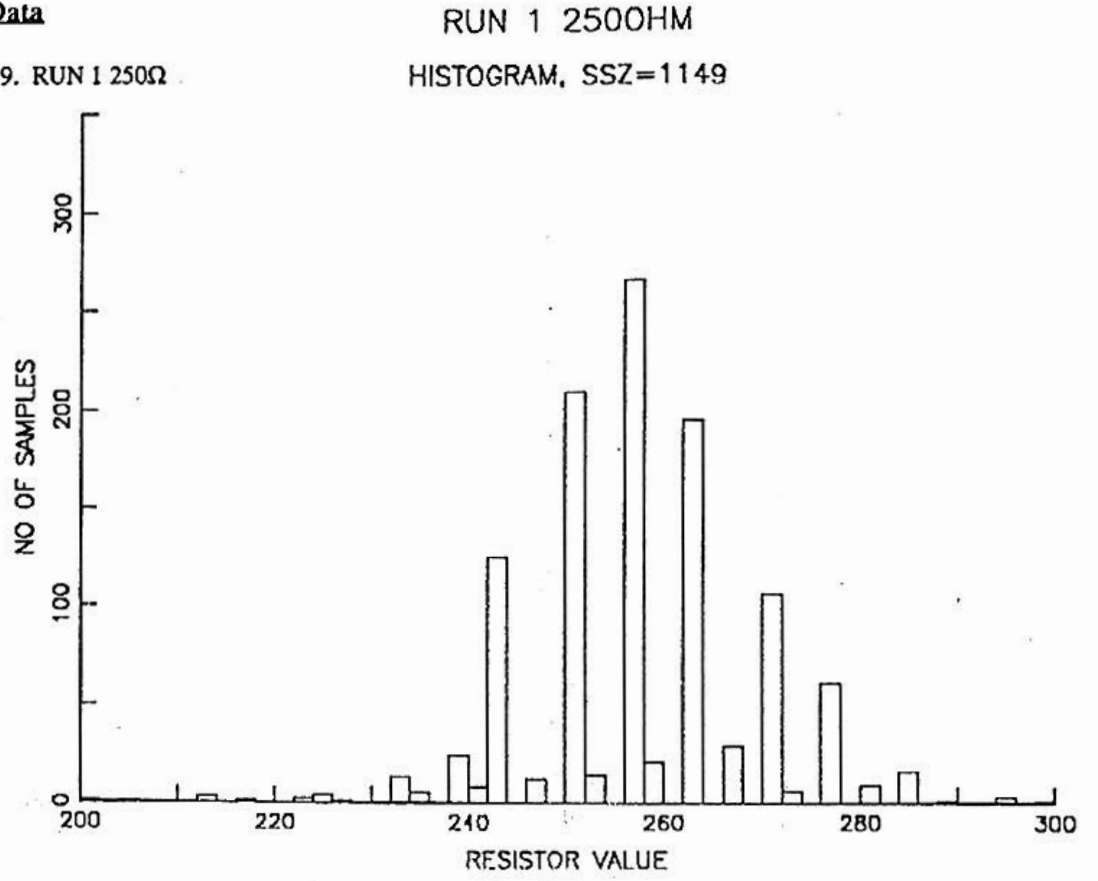
Test Data

Figure 8. RUN 5 100Ω



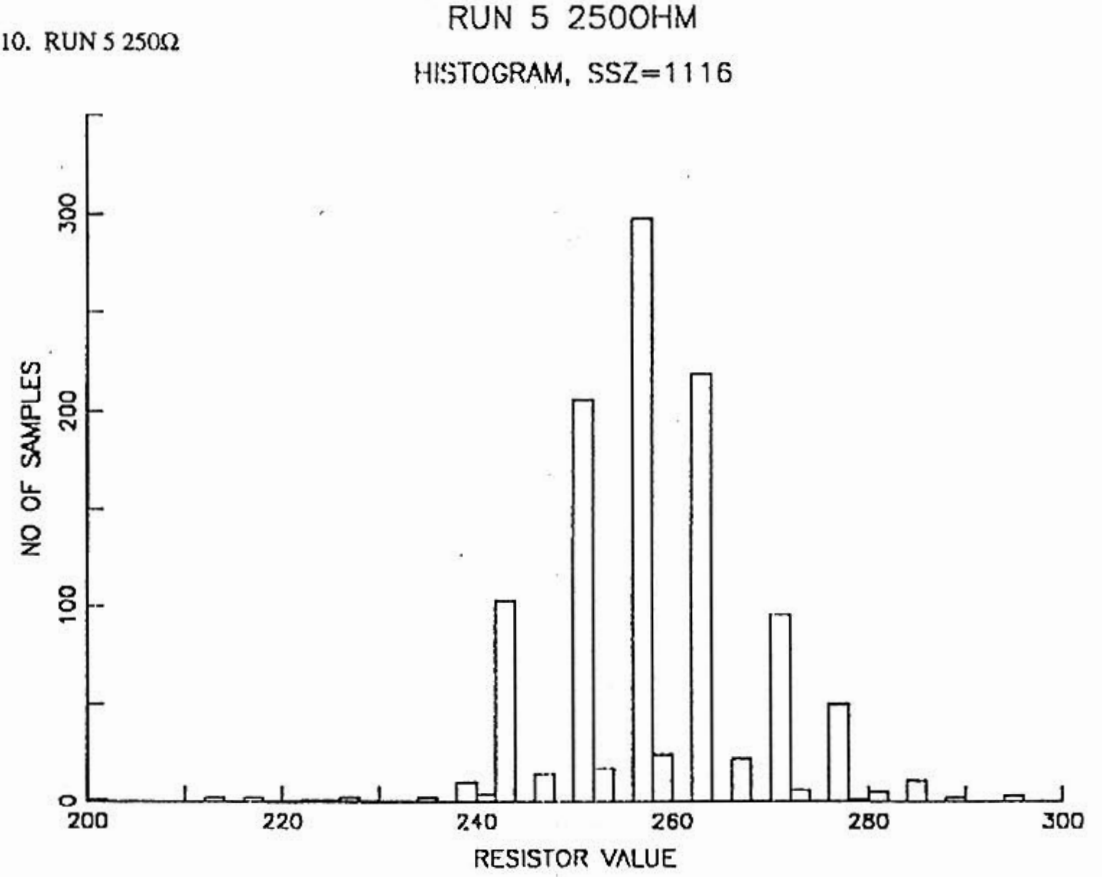
Test Data

Figure 9. RUN 1 250Ω



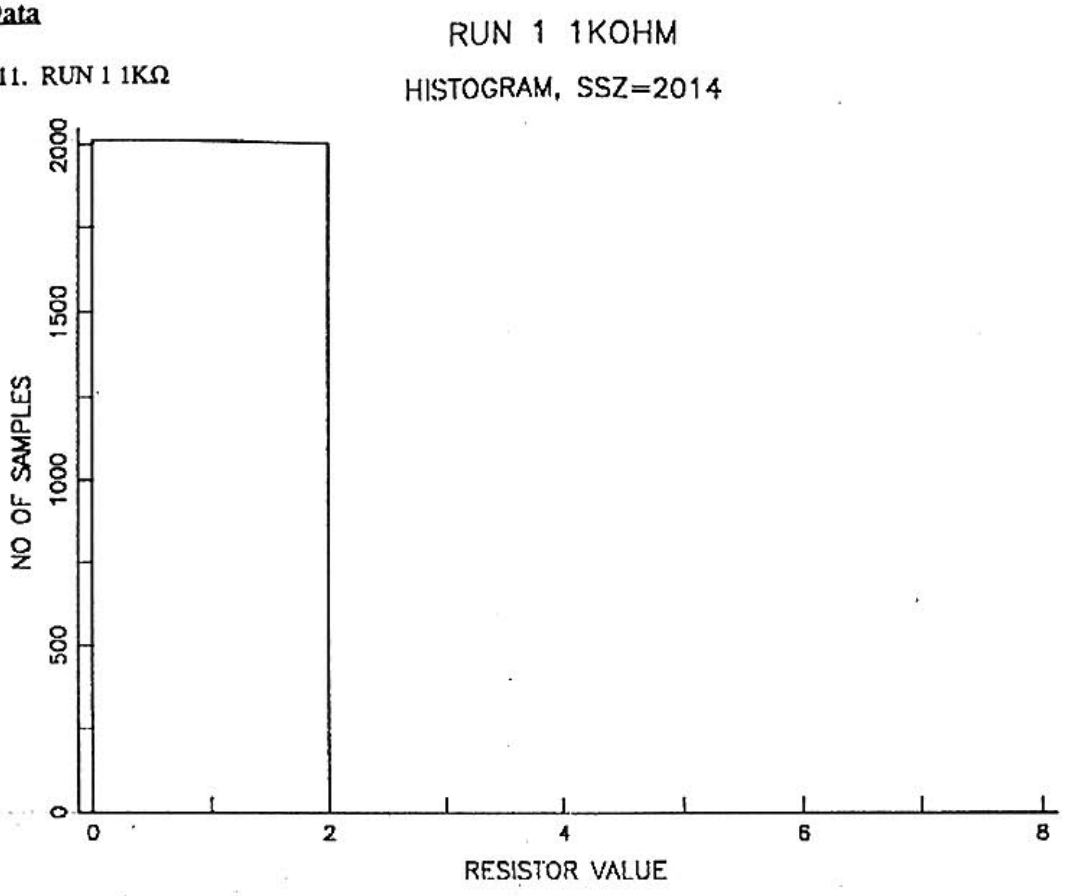
Test Data

Figure 10. RUN 5 250Ω



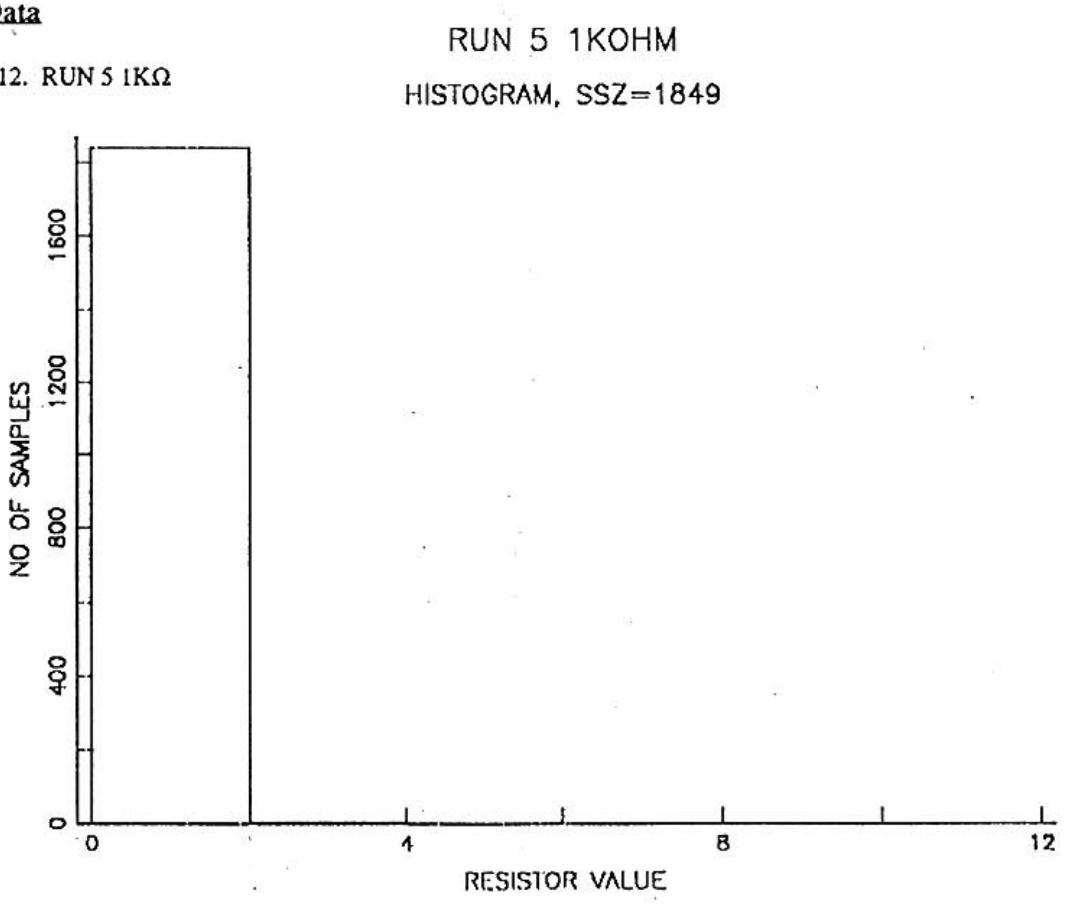
Test Data

Figure 11. RUN 1 1KΩ



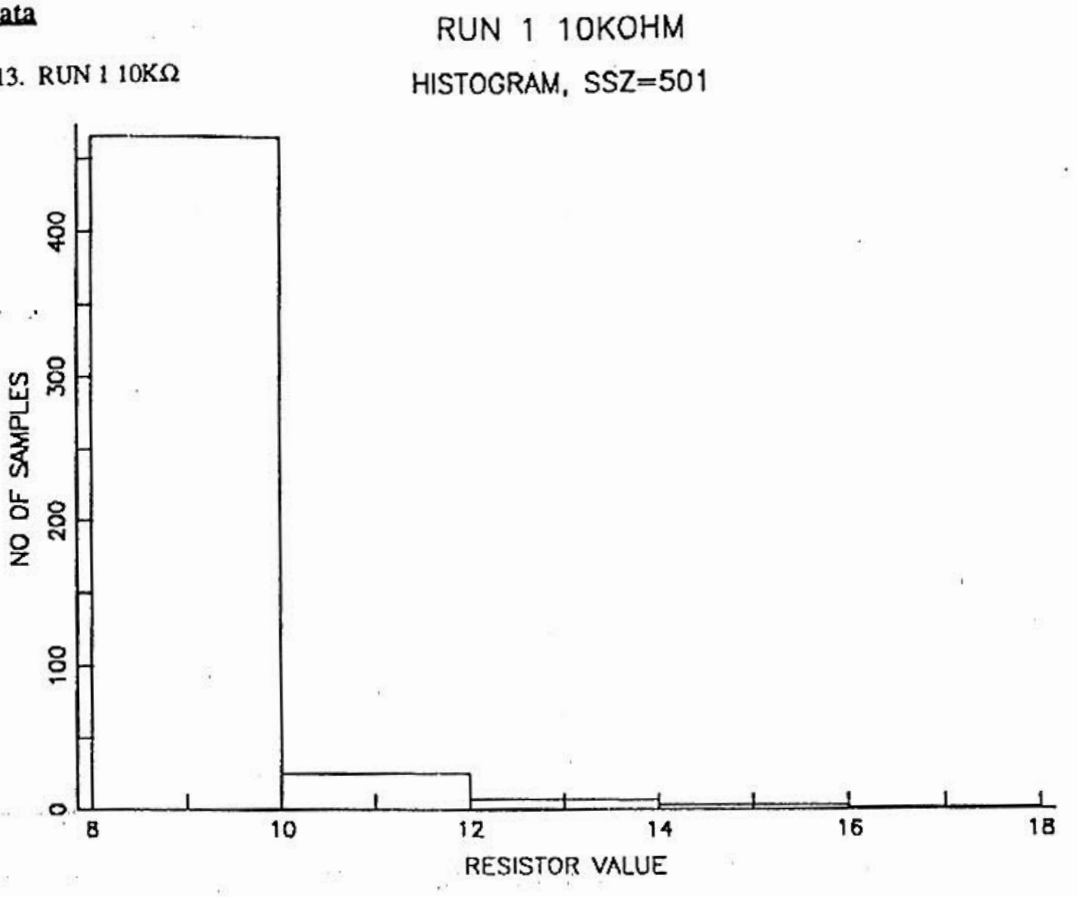
Test Data

Figure 12. RUN 5 1KΩ



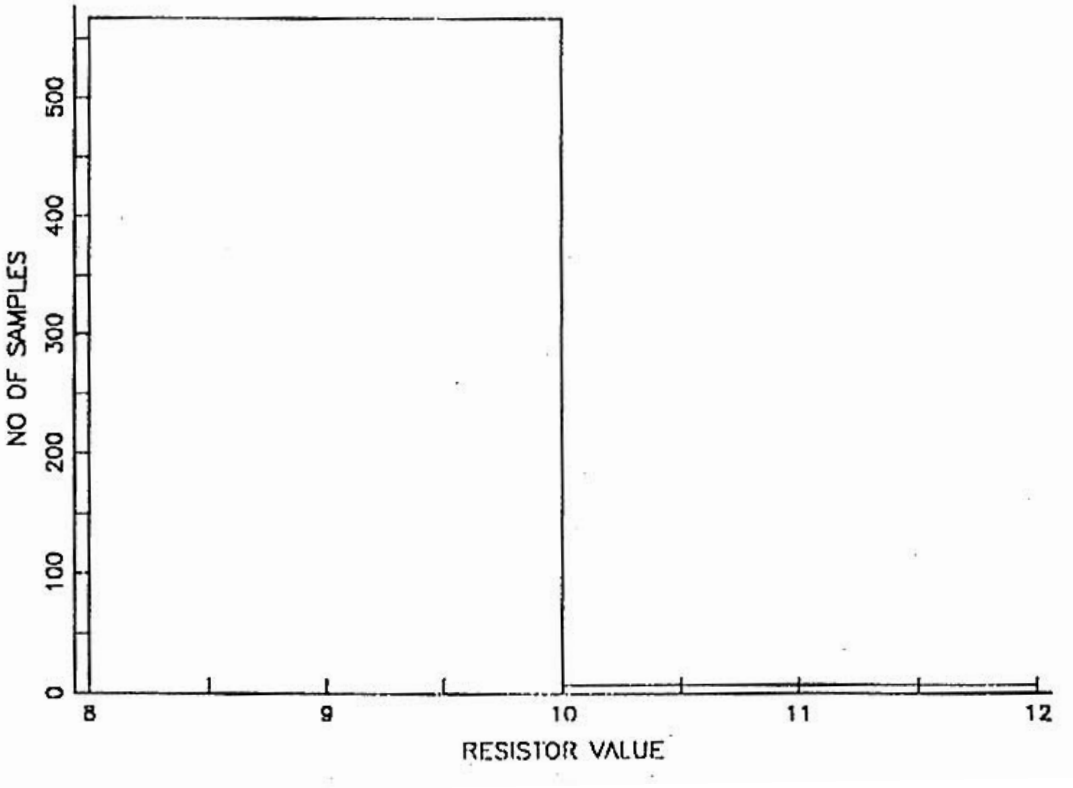
Test Data

Figure 13. RUN 1 10KΩ



Test Data

Figure 14. RUN 5 10KΩ



Power Rating

Report submitted by James Tso of Ohmega Technologies.

EXPT NO: 2-96 DATE: 1-20-96
RCM: 25 OHM/SQ (LAYER 4)
LAYERS: 6
SUBSTRATE: FR-4
ROOM TEMP: 70 DEG F

RESISTANCE			IBM PART NO.	SIZE	
UUT	OHMS	TYPE		W mils	L mils
R2	10	PARTIAL	rb10_25_30ly4_b	30	12
R3	100	BAR	rb100_25_15ly4_b	15	60
R4	100	BAR	rb100_25_10ly4_b	10	40
R5	250	BAR	rb250_25_20ly4_b	20	200
R6	250	BAR	rb250_25_10ly4_b	10	100
R7	250	BAR	rb250_25_5ly4_b	5	50
R8	4.7K	SERPENTINE	rb4_7_25_8ly4_s	8	
R9	4.7K	SERPENTINE	rb4_7_25_10ly4_s	10	

RESISTOR	Ω	V	mA	W
R2	9.692	.44	45.4	.02
R2	9.728	.5	51.4	.26
R2	9.690	.75	77.3	.058
R2	9.682	1.0	103.7	.104
R2	9.660	1.25	129.5	.162
R2	9.648	1.51	156.3	.236
R2	10.040	1.75	174.5 UNSTABLE	.306
R2	0	2	0 OPEN	0
R3	104.286	0	0	0
R3	104.555	1.01	9.66	.01
R3	104.499	2.04	19.56	.04
R3	104.549	3.01	28.8	.087
R3	104.167	4.0	38.4	.154
R3	103.934	5.02	48.35	.242
R3	103.793	6.02	58.0	.349
R3	103.693	7.02	67.7 UNSTABLE	.475
R3	0	8.04	0 OPEN	0
R4	106.527	0	0	0
R4	106.667	1.04	9.75	.01
R4	106.558	2.03	19.06	.039
R4	106.167	3.05	28.70	.087
R4	106.266	4.07	38.30	.156
R4	105.870	5.05	47.70 UNSTABLE	.241
R4	0	6.01	0 OPEN	0
R5	252.290	.97	3.85	.004
R5	252.658	2.04	8.09	.017
R5	252.676	3.02	11.96	.036
R5	252.475	4.08	16.16	.066
R5	252.520	5.01	19.84	.099
R5	251.822	6.22	24.70	.154
R5	252.128	7.11	28.20	.201
R5	254.275	8.03	31.58	.254
R5	252.101	9.00	35.70	.321
R5	252.109	10.16	40.30	.409

R5	251.701	11.10	44.10	.490
R5	251.660	12.13	48.20	.585
R5	251.923	13.10	52.00	.681
R5	251.699	14.07	55.90	.787
R5	251.500	15.09	60.00	.905
R5	251.487	16.07	63.90	1.027
R5	251.475	17.05	67.80	1.156
R5	251.108	18.13	72.20	1.309
R5	251.055	19.03	75.80	1.442
R5	251.177	20.27	80.70 UNSTABLE	1.636
R5	0	21.23	0 OPEN	0
R6	263.970	0	0	0
R6	264.565	2.10	7.93	.017
R6	264.212	4.09	15.48	.063
R6	263.203	6.08	23.10	.140
R6	263.312	8.11	30.80	.250
R6	262.827	10.04	38.20	.384
R6	262.771	12.14	46.20 UNSTABLE	.561
R6	0	14.07	0 OPEN	0
R7	259.630	0	0	0
R7	260.565	1.01	3.87	.004
R7	260.212	2.00	7.70	.015
R7	259.203	3.02	11.64	.035
R7	259.312	4.02	15.49	.062
R7	258.827	5.15	19.87	.102
R7	258.827	6.00	23.20	.139
R7	258.827	7.05	27.30	.192
R7	258.771	8.08	31.30 UNSTABLE	.253
R7	0	9.11	0 OPEN	0
R8	4842.100	0	0	0
R8	4936.212	5.03	1.02	.005
R8	4770.270	10.59	2.22	.024
R8	4855.346	15.44	3.18	.049
R8	4848.193	20.12	4.15	.083
R8	4852.713	25.04	5.16	.129

RESISTOR	Ω	V	mA	W
R2	34.94	0	0	0
R2	34.53	.25	7.24	.002
R2	35.25	.52	14.75	.008
R2	35.23	.75	21.4	.016
R2	35.18	1.07	30.3	.032
R2	35.17	1.25	35.6	.045
R2	35.12	1.50	42.80	.064
R2	34.66	1.75	50.60	.089
R2	35.04	2.04	58.10	.118
R2	34.96	2.26	64.50	.145
R2	34.72	2.60	74.80 . UNSTABLE	.194
R2	0	2.77	0 OPEN	0
R4	1056.57	0	0	0
R4	1058.73	2.00	1.89	.004
R4	1056.70	4.10	3.88	.016
R4	1055.46	6.09	5.77	.035
R4	1053.95	8.01	7.60	.061
R4	1051.20	10.06	9.57	.097
R4	1045.14	12.04	11.52	.139
R4	1041.39	14.09	13.53 UNSTABLE	.191
R4	0	16.60	0 OPEN	0
R5	1057.00	.0	.0	.0
R5	1057.59	2.02	1.91	.004
R5	1057.74	4.03	3.81	.015
R5	1093.36	6.09	5.57	.034
R5	1059.06	8.07	7.62	.061
R5	1057.47	10.12	9.57	.097
R5	1056.14	12.04	11.40	.137
R5	1054.60	14.10	13.37	.189
R5	1052.92	15.12	14.36	.217
R5	1051.67	16.08	15.29	.246
R5	1042.49	20.12	19.30	.388
R5	1041.87	21.15	20.30	.429
R5	1045.02	22.05	21.10 UNSTABLE	.465

R8	4846.635	30.97	6.39	.198
R8	4848.485	35.20	7.26	.256
R8	4844.125	40.40	8.34	.337
R8	4849.661	50.00	10.31	.516
R8	4843.373	60.30	12.45	.751
R8	4841.379	70.20	14.50	1.018
R8	4837.545	80.40	16.62	1.336
R8	4836.286	90.10	18.63	1.679
R8	4815.166	101.60	21.10	2.144
R8	4828.947	110.10	22.80	1.510
R8	4820.000	120.50	25.00	1.056
R8	4834.483	140.20	29.00 UNSTABLE	1.036
R8	0	160.50	0 OPEN	0
R9	4556.700	0	0	0
R9	4569.620	10.83	2.37	.026
R9	4570.787	20.34	4.45	.091
R9	4565.022	30.54	6.69	.204
R9	4555.809	40.00	8.78	.351
R9	4566.210	50.0	10.95	.548
R9	4562.453	61.00	13.37	.816
R9	4560.155	70.50	15.46	1.090
R9	4556.314	80.10	17.58	1.408
R9	4562.814	90.80	19.90	1.807
R9	4541.850	103.10	22.70	1.340
R9	4553.719	110.20	24.20	2.667
R9	4543.396	120.40	26.50	3.191
R9	4540.070	130.30	28.70	3.740
R9	4535.484	140.60	31.00	4.359
R9	4539.157	150.70	33.20	5.003
R9	4541.076	160.30	35.30	5.659
R9	4583.333	170.50	37.20 UNSTABLE	6.343
R9	0	180.50	0 OPEN	0

EXPT NO: 2-96 DATE: 1-23-96
RCM: 100 OHM/SQ (LAYER 2)
LAYERS: 6
SUBSTRATE: FR-4
ROOM TEMP: 70 DEG F

RESISTANCE			IBM PART NO.	SIZE	
UUT	OHMS	TYPE		W mils	L mils
R2	33	PARTIAL	rb33_100_30ly2_b	30	10
R4	1000	BAR	rb1K_100_5ly2_b	5	50
R5	1000	BAR	rb1K_100_10ly2_b	10	100
R6	1000	BAR	rb1K_100_20ly2_b	20	200
R8	10K	SERPENTINE	rb10K_100_5ly2_s	5	
R9	10K	SERPENTINE	rb10K_100_10ly2_s	10	

R8	9698.60	90.10	9.29 UNSTABLE	.837
R8	0	95.1	0 OPEN	0
R9	9887.40	0	0	0
R9	9962.96	10.76	1.08	.012
R9	9911.76	20.22	2.04	.041
R9	9903.23	30.70	3.10	.095
R9	9900.99	40.00	4.04	.162
R9	9882.12	50.30	5.09	.256
R9	9884.87	60.10	6.08	.365
R9	9887.17	70.10	7.09	.497
R9	9865.20	80.50	8.16	.657
R9	9858.23	90.40	9.17	.829
R9	9833.98	100.70	10.24	1.031
R9	9804.10	110.10	11.23	1.236
R9	9771.99	120.00	12.28	1.474
R9	9790.10	130.60	13.34 UNSTABLE	1.742
R9	0	140.00	0 OPEN	0

APPENDIX C. REFERENCES

1. Klaiber, Robert et all., "Critical Issues Packaging", Circuits Assembly, December 1995, pp. 30 - 33.
2. Mahler, Bruce, "Planar Resistor Technology in High Density MLB Applications", Printed Circuit Fabrication, June 1985, pp.154 - 167.
3. Tso, James, "Ohmega Technologies, Inc. Design Guide"
4. Peeters, Joris et all., "Characterization of Integrated Resistors for Broadband Telecom Printed Circuit Board".
5. "Ohmega-Ply® Cost Analysis", April 14, 1993 letter from Ohmega Technologies, Inc.